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CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

Y EV2p9 Schematic

Title: Table of Contents	
Engineer: Surface	
Size: A3	Project Name: Y -- EV 2.9
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Schematics Change History

Rev.	Date	Comments
Op9	28 Oct 2014	<ol style="list-style-type: none"> Starting with G_EV1_1021-1630.DSN Added SL schematic from page 72 ...\\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN Added External USB3 schematic from ...\\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN Added external DP ...\\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN Added IR_CAMERA from Front Camera...put in page 49 Removed page 73 PCIE GPU Added Blade from T Removed P72 T2B Pwr Transistors
Op10	3 Nov 2014	<ol style="list-style-type: none"> Changing to NVDC Replaced GTX with GT, kept bypass caps Replaced Charger with BQ24770
Op11	3 Nov 2014	<ol style="list-style-type: none"> Replace SKL-U with SKL-Y
Op12	11 Nov 2014	<ol style="list-style-type: none"> Model DDR connection from Intel SDS
Op13	18 Nov 2014	<ol style="list-style-type: none"> Added FUB information to all components Changed Decretes.. sizing caps
Op14	20 Nov 2014	<ol style="list-style-type: none"> Added +5VA_SHA Added T Cost Down/XCN's Added SL +5V load Switch & Caps Added Blade +5V load Switch & Caps
Op15	26 Nov 2014	<ol style="list-style-type: none"> Removed Boost Re-adjusted usb ports on CPU Removed Audio DSP
Op16	03 Dec 2014	<ol style="list-style-type: none"> changed +1VSB regulator changed IR Camera/added diode added power numbers from 0.91 PDG, Oct14 changed BLADE connector cpu decoupling caps changed changed +5V/+3V inductors (place holder)
Op17	05 Dec 2014	<ol style="list-style-type: none"> swapped M_A_CAA with MA_CAB on U1601/U1602 added two SAR chips, P32 remove tp's from csi lines on (p23) change from 10 ceramic to 3 tantalum-poly on usb3 typeA (p45) remove the RSENSE from output of +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) change RSENSE input to 0402 from 0603 for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) input regulator change inductor for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58) to HMLE20161B-1R0MDR-01 change RSENSE input to 0402 from 0603 for +5V_TS,+5V_SDXC,+5V_AUDIO,+5V,+5V_FAN(p64) change RSENSE input to 0402 from 0603 for +3P3V_PANEL,+3P3V,+3P3V_SENSOR,+1P8V_DMIC (p65) Replacing the SL connector with X908351-001 Replace PL5901 and PL5902 with CMLE042T-2R2MS-01 Replace 0402 1uF 6.3V with 0201 1uF 6.3V X5R Replace L7201 with TOKO #A919CY-100M Added VSYS -> BLADE FANG supply (p73)
Op18	09 Dec 2014	<ol style="list-style-type: none"> Reduced sizes of parts for Cameras (Resistors/Caps/Regulators)
Op19	12 Dec 2014	<ol style="list-style-type: none"> All 47uF caps become 0805/1mmZ All 10uF caps become 0402...4V/6.3V
Op20	15 Dec 2014	<ol style="list-style-type: none"> changed SAM flash to reduce size to 2x3 from 5x4 Shui Changes more Shui Changes
Op21	16 Dec 2014	<ol style="list-style-type: none"> changed SAM flash to reduce size to 2x3 from 5x5 changes from EV_schematic_issue_check_1216_JDM1.xlsx changed name of +6_12 to +V_ALWAYS_ON Removed 2 Mikes & Front Mike & added FPC conn Added 2nd BLADE connector
Op22	17 Dec 2014	<ol style="list-style-type: none"> Replaced SD connector with AY531465T changes from EV_schematic_issue_check_viola_1217_JDM1.xlsx
Op23 current		<ol style="list-style-type: none"> See apexUfixes_revXpXX.xlsx

CAD Note:

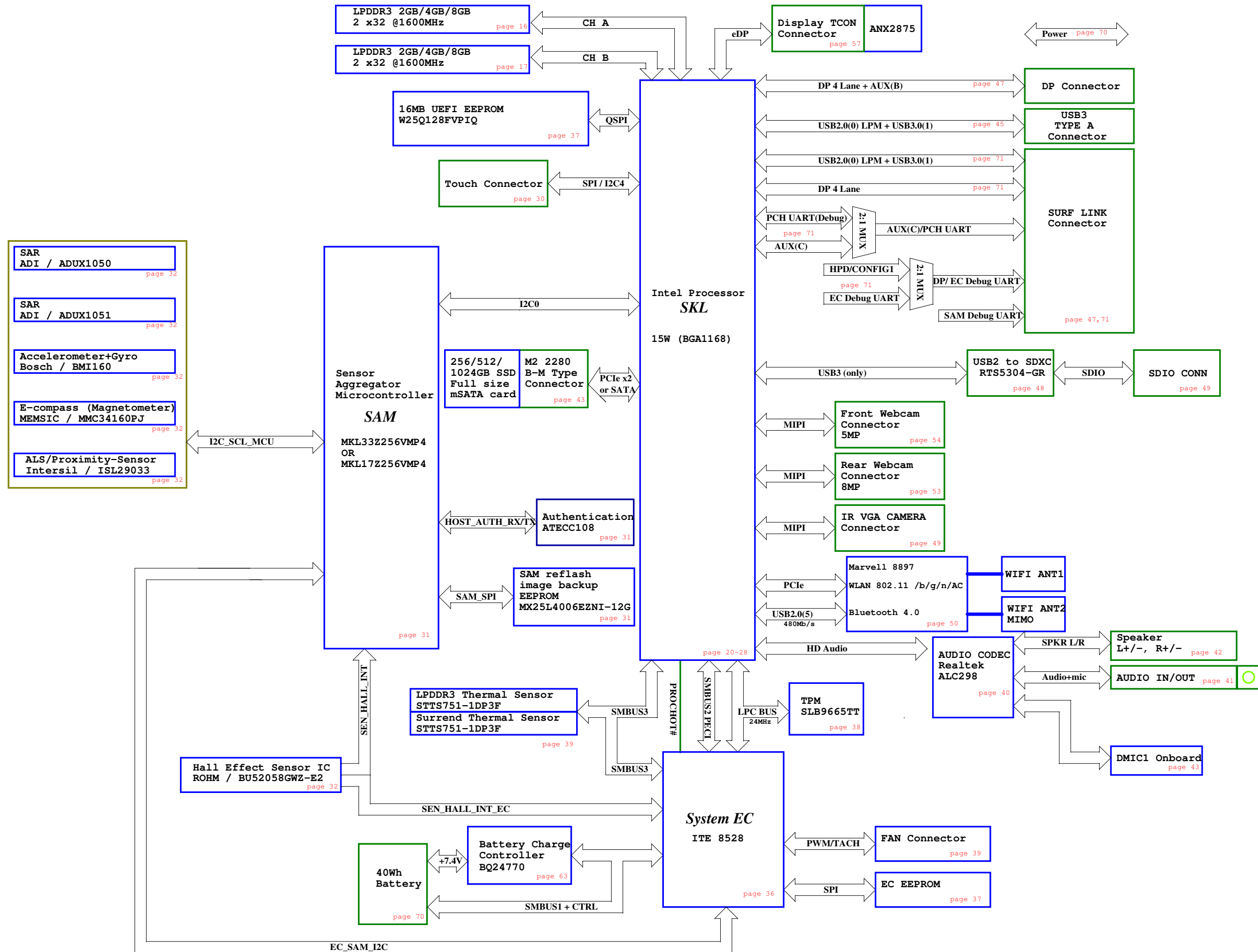
Default component footprint is SMD 0201, X5R, 1% resistors

S = Short after design fixed

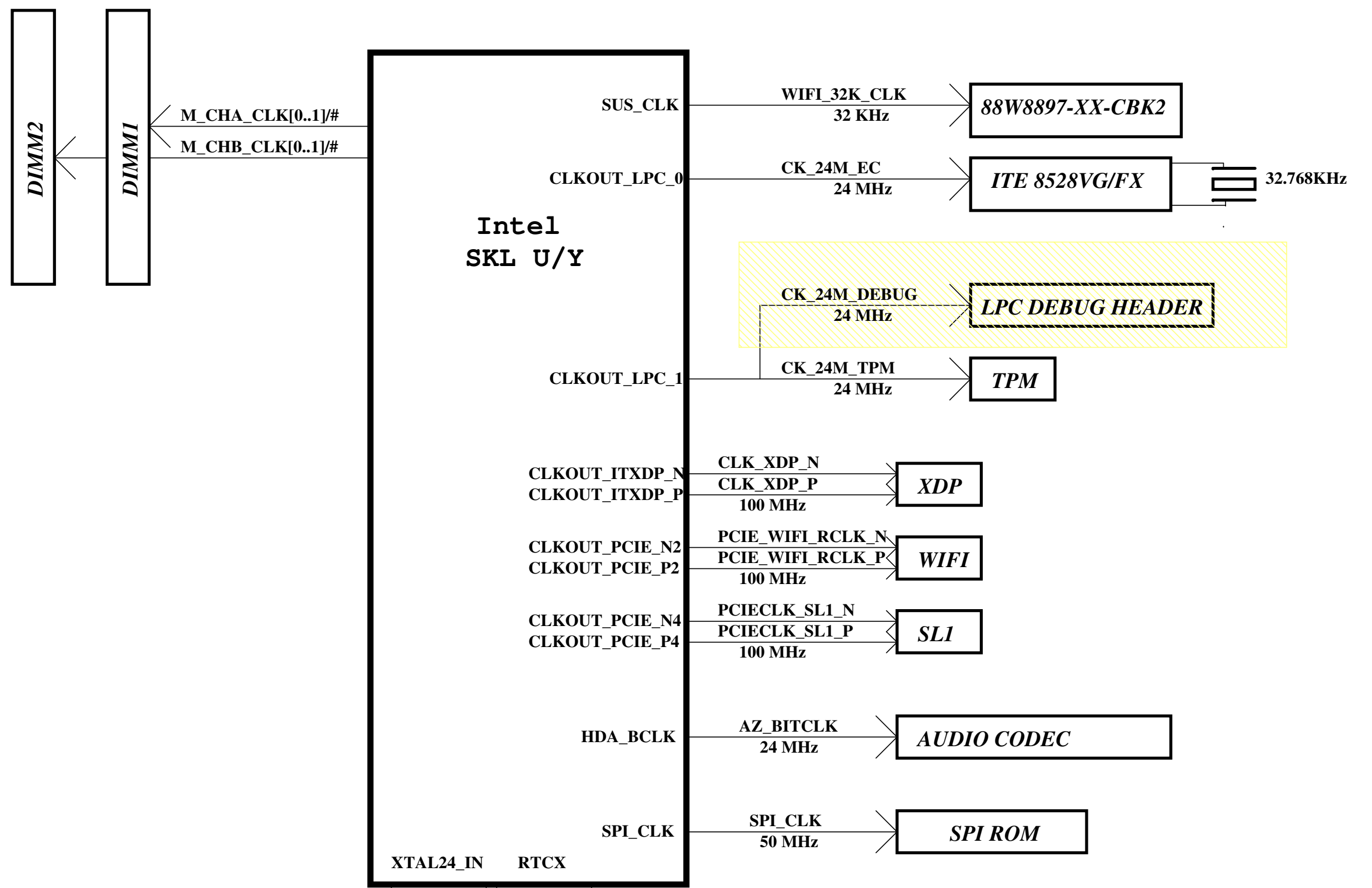
Property: BUILD-OPT

DNP = Not Installed Part.

Title: CHANGE HISTORY-1	
Engineer: Surface	
Size A3	Project Name Y -- EV 2.9
Date: Friday, July 17, 2015	Rev 2.9.0
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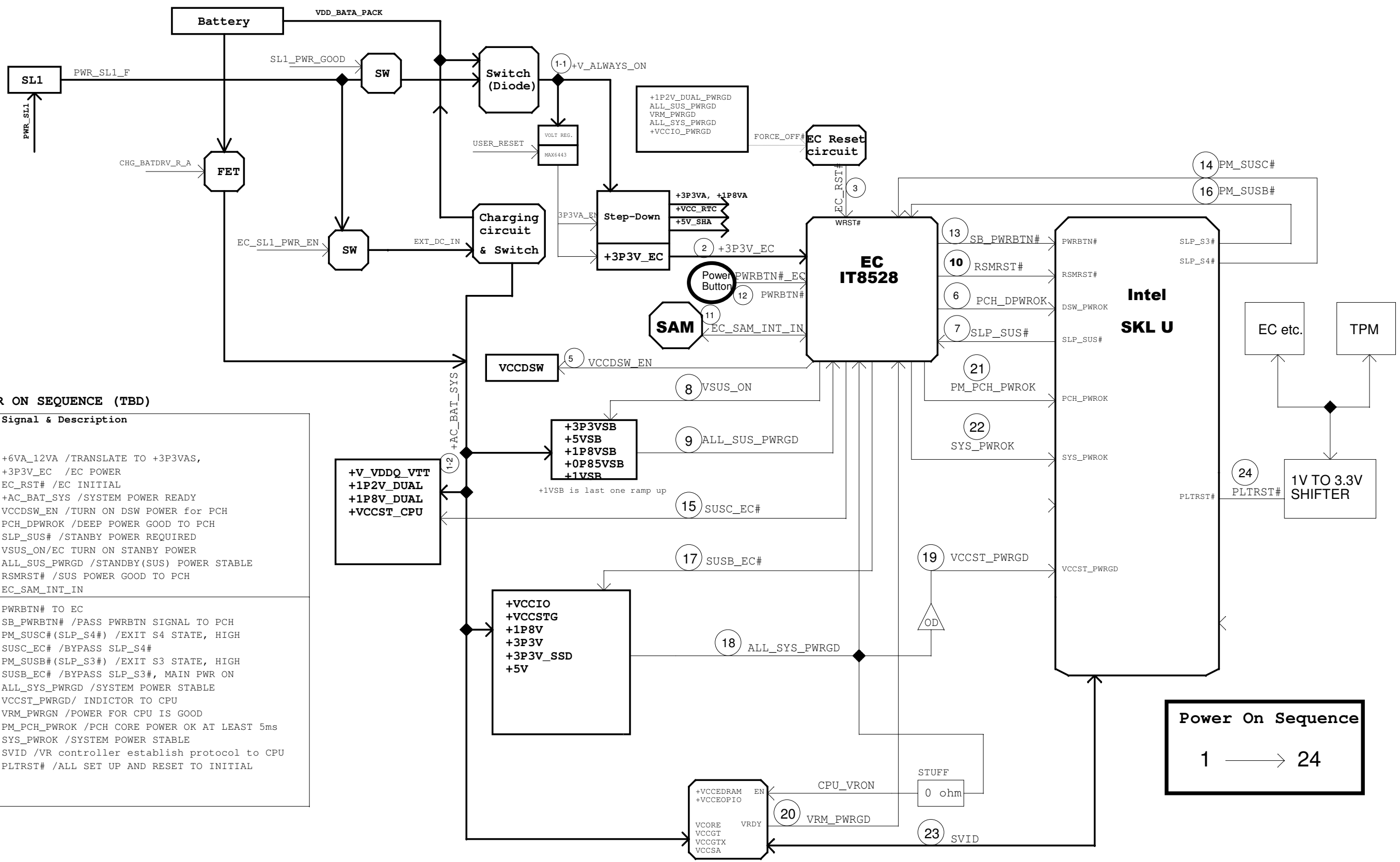


HSW Buffer Through Mode for Pre-Silicon



Y EV2p9 Schematic

Title: CLOCK DISTRIBUTION(TBD)		
Microsoft		Engineer: Surface
Size A3	Project Name Y -- EV 2.9	Rev 2.9.0
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POWER ON SEQUENCE (TBD)

STEP	Signal & Description
1	+6VA_12VA /TRANSLATE TO +3P3VAS,
2	+3P3V_EC /EC POWER
3	EC_RST# /EC INITIAL
4	+AC_BAT_SYS /SYSTEM POWER READY
5	VCCDSW_EN /TURN ON DSW POWER for PCH
6	PCH_DPWRK /DEEP POWER GOOD TO PCH
7	SLP_SUS# /STANBY POWER REQUIRED
8	VSUS_ON/EC TURN ON STANBY POWER
9	ALL_SUS_PWRGD /STANDBY(SUS) POWER STABLE
10	RSMRST# /SUS POWER GOOD TO PCH
11	EC_SAM_INT_IN
12	PWRBTN# TO EC
13	SB_PWRBTN# /PASS PWRBTN SIGNAL TO PCH
14	PM_SUSC#(SLP_S4#) /EXIT S4 STATE, HIGH
15	SUSC_EC# /BYPASS SLP_S4#
16	PM_SUSB#(SLP_S3#) /EXIT S3 STATE, HIGH
17	SUSB_EC# /BYPASS SLP_S3#, MAIN PWR ON
18	ALL_SYS_PWRGD /SYSTEM POWER STABLE
19	VCCST_PWRGD/ INDICATOR TO CPU
20	VRM_PWRGN /POWER FOR CPU IS GOOD
21	PM_PCH_PWRK /PCH CORE POWER OK AT LEAST 5ms
22	SYS_PWRK /SYSTEM POWER STABLE
23	SVID /VR controller establish protocol to CPU
24	PLTRST# /ALL SET UP AND RESET TO INITIAL

Power On Sequence
1 → 24