Table of Contents

CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

W x H 457 x 296 mm

<Variant Name>

Title: Table of Contents

Engineer: <OrgAddr1>

Size: Custom | Project Name: KBL M DV1p0 | Rev: 1.00

Date: Tuesday, December 13, 2016 | Sheet 1 of 76

BUILD-OPT	BOM Assy	Remarks
ALL	Common	DEFAULT - Populated as shown in Core schematic for all variants
DNP	Common	O-STUFF for all variants
TBL1001	Common	CPU selection (In Common; No SOC based variants)
TBL3602	Common	Res Jumpers (In Common; No SOC based variants)
U23E	Common	Only populated to support U23e variants (In Common; No SOC based variants)
TBL2301	Bd ID	Res Jumpers
TBL3601	BdID	Res Jumpers
TBL1601	Mem	LPDDR3 Memory Assembly Options
TBL3801	TPM	Security Device Options
TBL4301	SSD	SSD Memory part options
SSD1	SSD	Only populated for single SSD configurations.
SSD2	SSD	Only populated for dual SSD configurations.
S	Debug	Legacy - Originally intended same as DBG_S. please replace with DBG_S, DBG_R, or DBG_D as appropriate.
DBG	Debug	Legacy - Same as DBG_D shown below. Part depopulated for MP.
DBG_D	Debug	Debug Part - Remove from BOM (Depopulate) for MP
DBG_N	Debug	Non-Debug Part - Installed only in non-debug builds
DBG_R	Debug	Debug Part - Replace with lower cost component for MP (Ex; replace precision shunt with 0-ohm jumper)
DBG_S	Debug	Debug Part - Replace with board short for MP (not commonly used anymore)
DBG_T	Debug	Debug Part - Used for Power Telemetry in MP as needed.
XDP	XDP	Legacy - Same as XDP_D
XDP_D	XDP	Only used as needed for CPU Debug. Depopulated for MP and most EV/DV/PV assemblies.
FAN	FAN	Parts used to support Fan option.

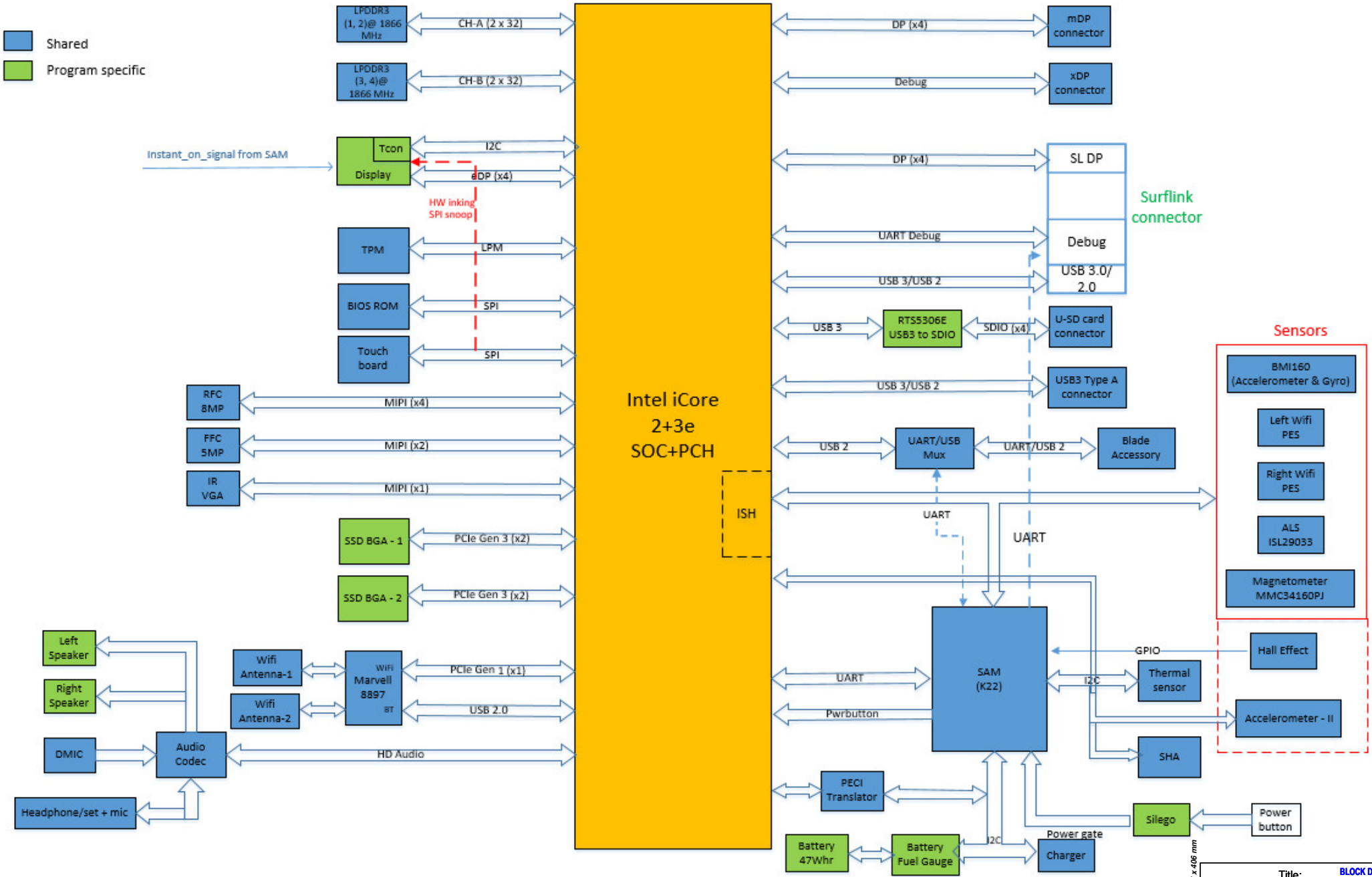
Allowable Part Substitutions

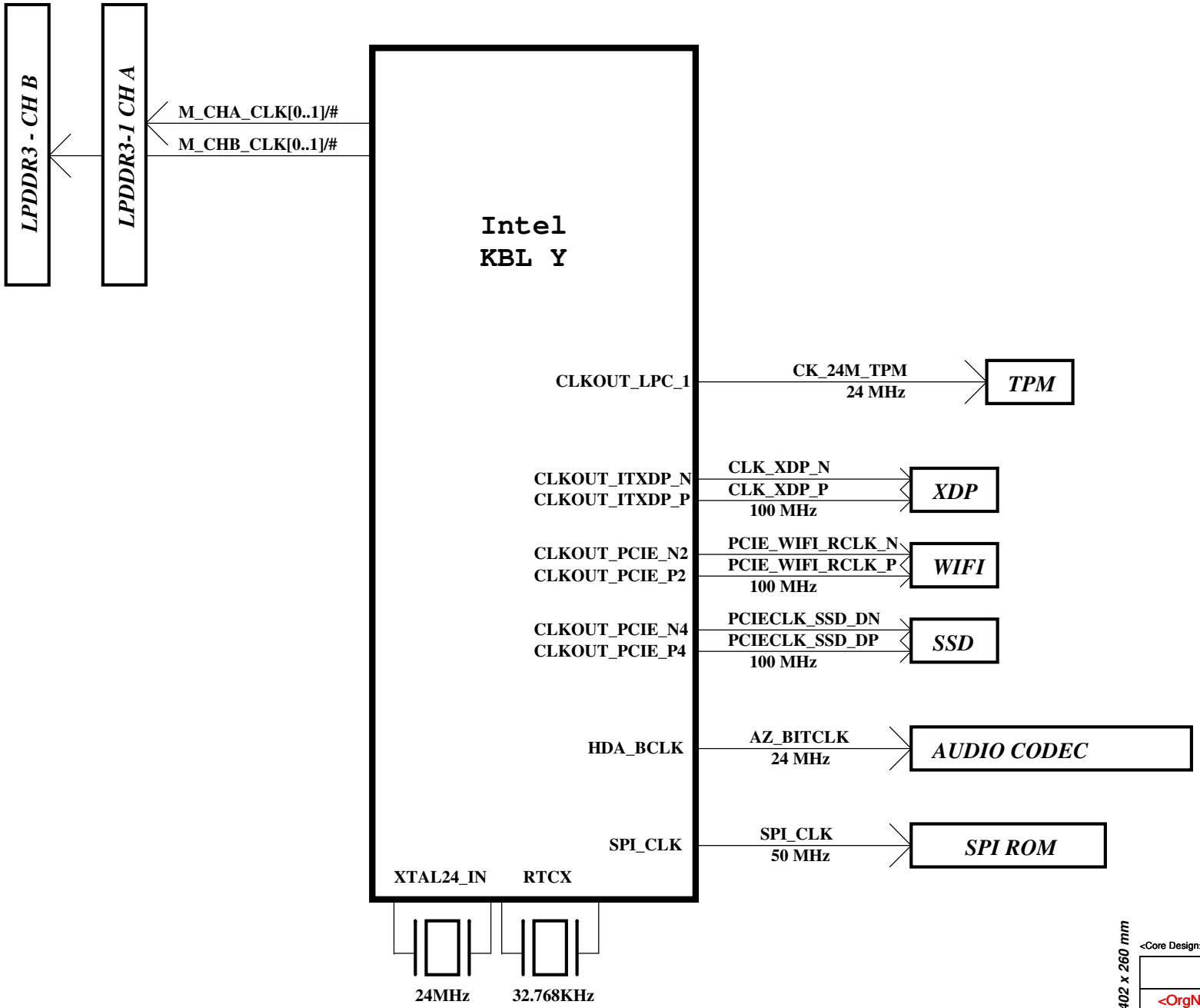
Primary Part	Primary Part Description	Substitute Part	Substitute Part Description	Reference Designator
X910478-001	CAP-POLY-TANT,SM,47 uF,16 V,20%,200 mOHM,1210	X944915-001	CAP-POLY-TANT,SM,47 uF,16 V,20%,90 mOHM,1210	C6334,C6335,C6351,C6352
X950699-001	IND-FER-COMMON MODE,SM,160 mA,25%,50 OHM,0504	X869713-001	IND-FER-COMMON MODE,SM,100 mA,25%,80 OHM,100MHZ,1.5DCR,1.25X1.0X.3MM	L4501,L4502,L4702,L4703,L4704,L4705, L4801,L4802,M71L1,M71L2
M1006065-001	IND,COMMON MODE,100mA,SURFACE MOUNT,90 OHM,2 LINE	X888388-001	IND-FER-COMMON MODE,SM,100 mA,20%,90 OHM,100MHZ,0302,NOT FOR NEW DESIGN	L4905,L4906,L5301,L5302,L5303,L5304, L5305,L5401,L5402,L5403
X911507-001	IND-PWR,SM,10 uH,2.5 A,154 mOHM,20%,5.4X5.2X1.8MM	M1002310-001	IND,POWER MULTILAYER,10uH,2.6A,20%,145mOhm,SURFACE MOUNT,5P4*5P2MM	L7204
X865865-001	TRA-N-CNL,SM,VMT3,20 V,200 mAmp,8 V	X885388-001	TRA-N-CNL,SM,2-L1B,20 V,250 mAmp,10 V,SSM3K37MFV	PQ5506,PQ7505,Q2002,Q2101,Q2102, Q2501,Q2502,Q3001,Q3004,Q4301, Q4701,Q5301,Q5401,Q5702,Q6306, Q6307,Q7000,Q7102,Q7201,Q1001
X861507-001	RES-FXD,SM,49.9 OHM,1%,1/20W,0201	X878664-001	IC,SM,WLCSP4,TPS22908YZTR,LOAD SWITCH	R1004,R1022,R1023,R1024,R1025,R1026, R1027,R1029,R1507,R2231,R2241,R6606, R6617

CAD Note:
Defaults: Footprint SMD 0201, Cap tmp Coeff X5R, 1% resistors

W x H 432 x 280 mm

Title: Build Options
Engineer: <OrgAddr1>
Size: Custom | Project Name: KBL M DV1p0 | Rev: 1.00
Date: Tuesday, December 13, 2016 | Sheet 2 of 76


Shared
Program specific
LPDDR3 (1, 2)@ 1866 MHz
CH-A (2 x 32)
LPDDR3 (3, 4)@ 1866 MHz
CH-B (2 x 32)
Instant_on_signal from SAM
Tcon
Display
I2C
eDP (x4)
HW inking
SPI snoop
TPM
LPM
BIOS ROM
SPI
Touch board
SPI
RFC 8MP
MIPI (x4)
FFC 5MP
MIPI (x2)
IR VGA
MIPI (x1)
SSD BGA - 1
PCIe Gen 3 (x2)
SSD BGA - 2
PCIe Gen 3 (x2)
Left Speaker
Right Speaker
DMIC
Audio Codec
Headphone/set + mic
Wifi Antenna-1
Wifi Antenna-2
WiFi Marvell 8897 BT
PCIe Gen 1 (x1)
USB 2.0
HD Audio
Intel iCore 2+3e SOC+PCH
ISH
DP (x4)
mDP connector
Debug
xDP connector
DP (x4)
SL DP
Surflink connector
Debug
UART Debug
USB 3/USB 2
USB 3.0/ 2.0
USB 3
RTS5306E USB3 to SDIO
SDIO (x4)
U-SD card connector
USB 3/USB 2
USB3 Type A connector
USB 2
UART/USB Mux
UART/USB 2
Blade Accessory
UART
UART
Sensors
BMI160 (Accelerometer & Gyro)
Left Wifi PES
Right Wifi PES
ALS ISL29033
Magnetometer MMC34160PJ
GPIO
Hall Effect
UART
Pwrbutton
SAM (K22)
I2C
Thermal sensor
Accelerometer - II
SHA
PECI Translator
Silego
Power button
Power gate
I2C
Battery 47Whr
Battery Fuel Gauge
Charger
W x H 627 x 406 mm
Title: BLOCK DIAGRAM
<OrgName>
Engineer:
<OrgAddr1>
Size: Custom
Project Name: KBL M DV1p0
Rev: 1.00
Date: Tuesday, December 13, 2016
Sheet 3 of 76



W x H 402 x 260 mm

<Core Design>

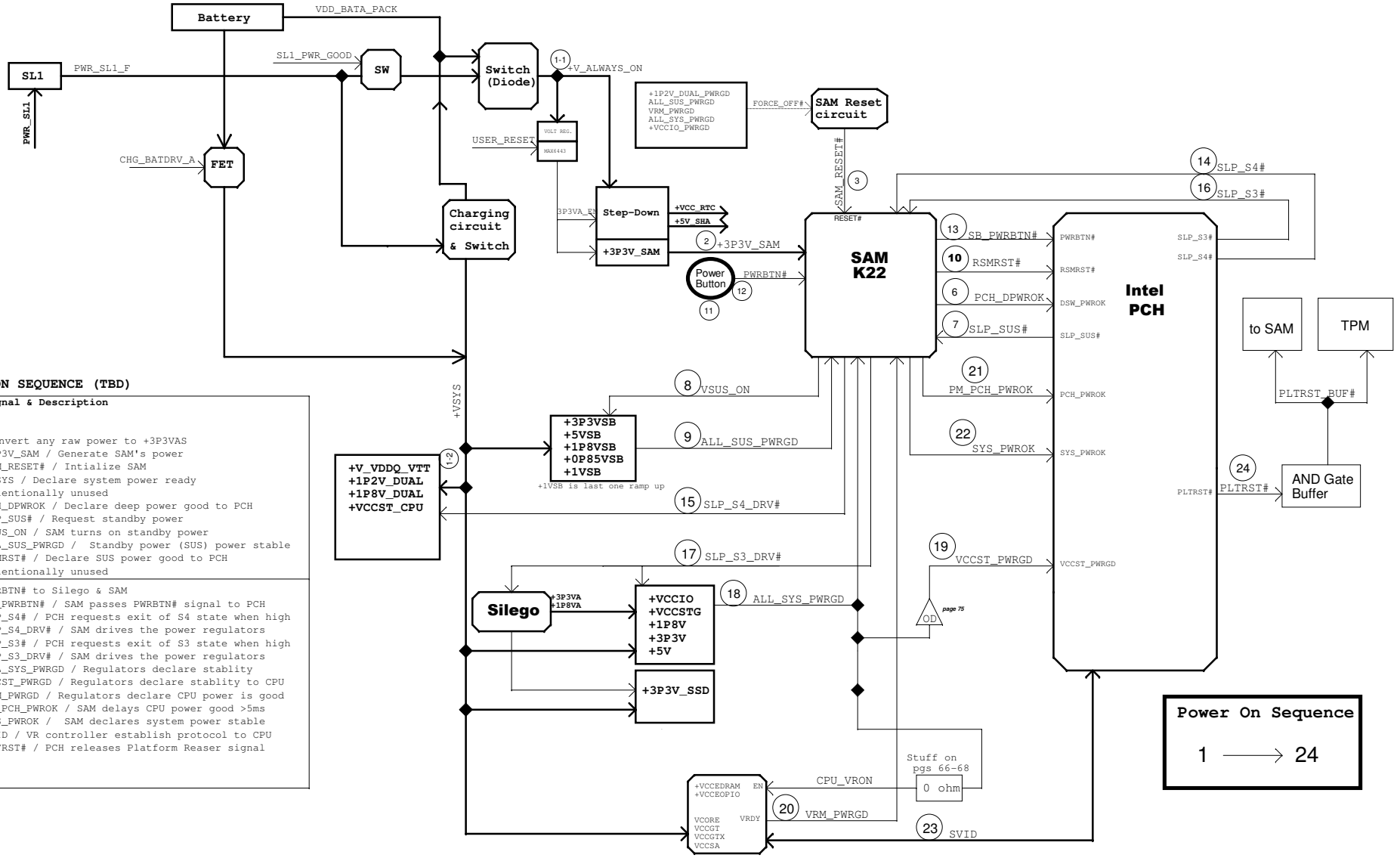
Title: CLCOK DISTRIBUTION

<OrgName> Engineer: <OrgAddr1>

Size: Custom | Project Name: KBL M DV1p0 | Rev: 2.89.6

Date: Tuesday, December 13, 2016 | Sheet 4 of 76

SIGNAL & RESET MAP



POWER ON SEQUENCE (TBD)

STEP	Signal & Description
1	Convert any raw power to +3P3VAS
2	+3P3V_SAM / Generate SAM's power
3	SAM_RESET# / Intialize SAM
4.	+VSYS / Declare system power ready
5.	Intentionally unused
6.	PCH_DPWROK / Declare deep power good to PCH
7.	SLP_SUS# / Request standby power
8.	VSUS_ON / SAM turns on standby power
9.	ALL_SUS_PWRGD / Standby power (SUS) power stable
10.	RSMRST# / Declare SUS power good to PCH
11.	Intentionally unused
12	PWRBTN# to Silego & SAM
13.	SB_PWRBTN# / SAM passes PWRBTN# signal to PCH
14.	SLP_S4# / PCH requests exit of S4 state when high
15.	SLP_S4_DRV# / SAM drives the power regulators
16.	SLP_S3# / PCH requests exit of S3 state when high
17.	SLP_S3_DRV# / SAM drives the power regulators
18.	ALL_SYS_PWRGD / Regulators declare stablity
19.	VCCST_PWRGD / Regulators declare stablity to CPU
20.	VRM_PWRGD / Regulators declare CPU power is good
21.	PM_PCH_PWROK / SAM delays CPU power good >5ms
22.	SYS_PWROK / SAM declares system power stable
23.	SVID / VR controller establish protocol to CPU
24.	PLTRST# / PCH releases Platform Reaser signal

W x H 654 x 422 mm
<Core Design>
Title: SIGNAL&RESET MAP
<OrgName> Engineer: <OrgAddr1>
Size: Custom | Project Name: KBL M DV1p0 | Rev: 1.00
Date: Tuesday, December 13, 2016 | Sheet 5 of 76