NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

CAMELLIA_15W

MV

2020.06.15

Marking	Description
I	Install
NI	Non-install
PROTO	Proto type
MP	Mass Production
TAA	Install for TAA
CRITICAL	Critical Parts

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK	EXIN LIN		
APPROVAL	MORRIS CHANG		
FILE NAME	CAMELLIA_15W_MV_MB_A01		
PCB P/N	60.XXXXX.XXXX	PCB VER	XXX

INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
	MAIN BOARD

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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DATE	CHANGE NO.	REV
21-OCT-2002		

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SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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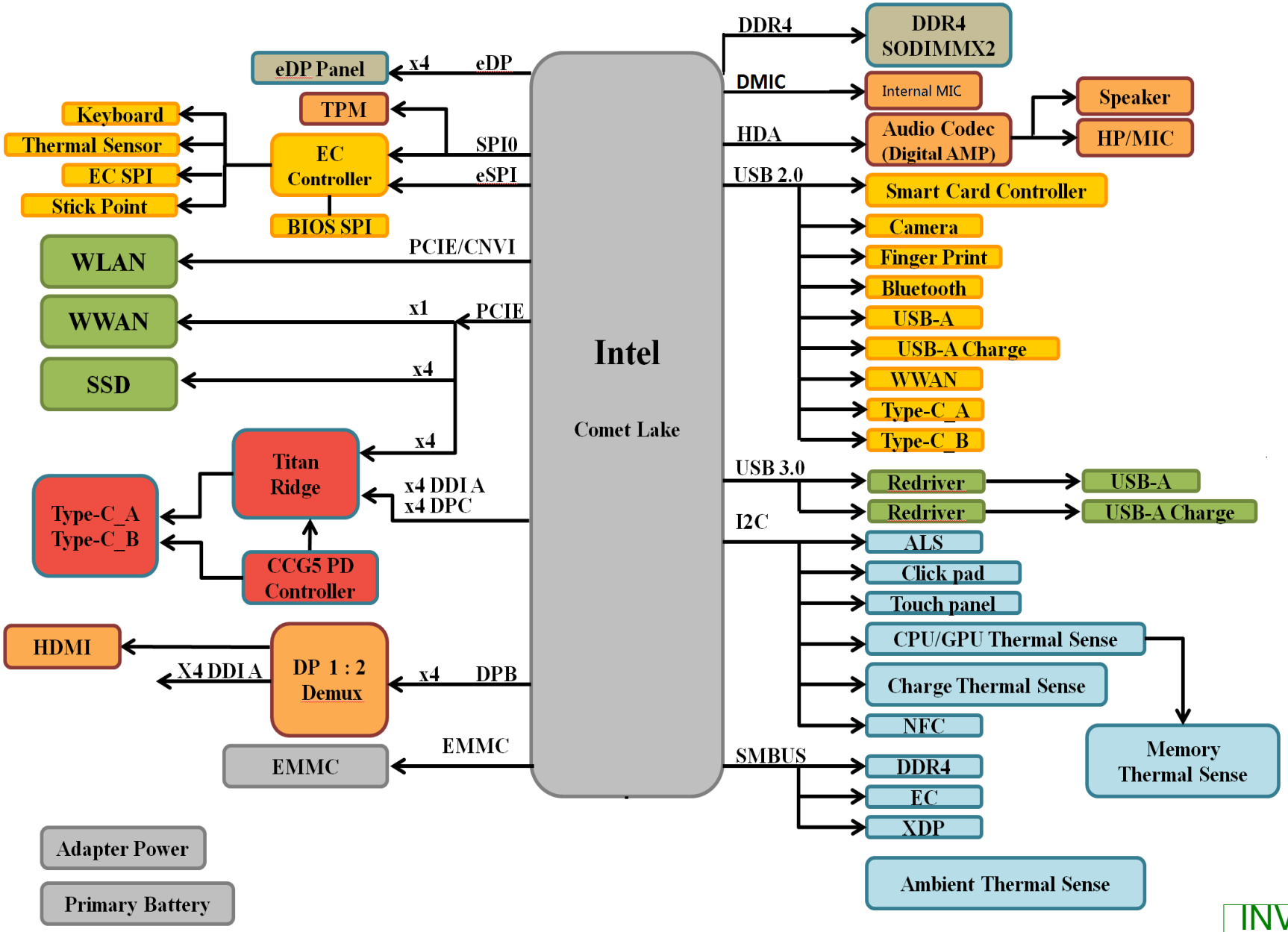
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



100% TO 45%

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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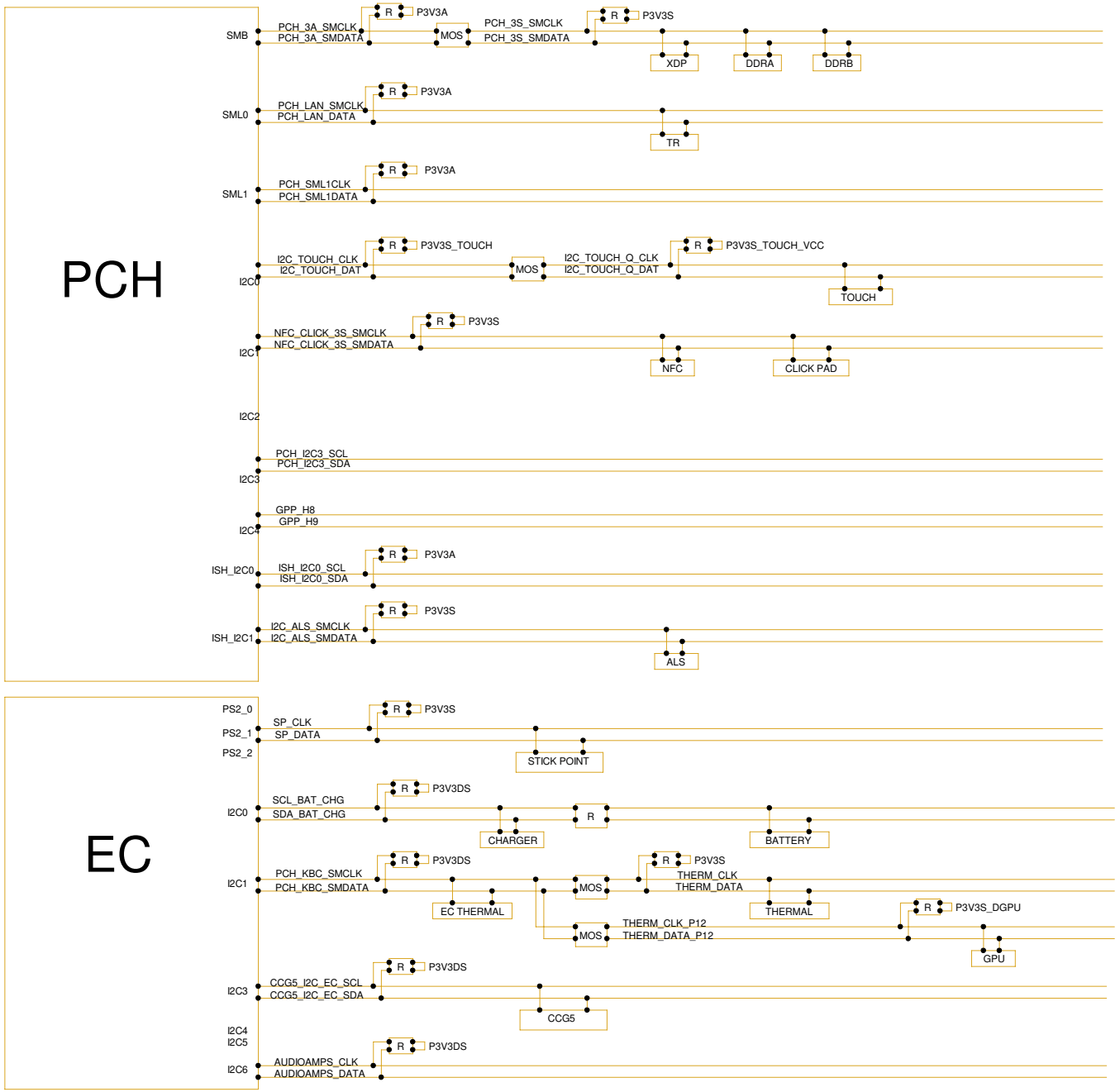
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
POWER BLOCK DIAGRM

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

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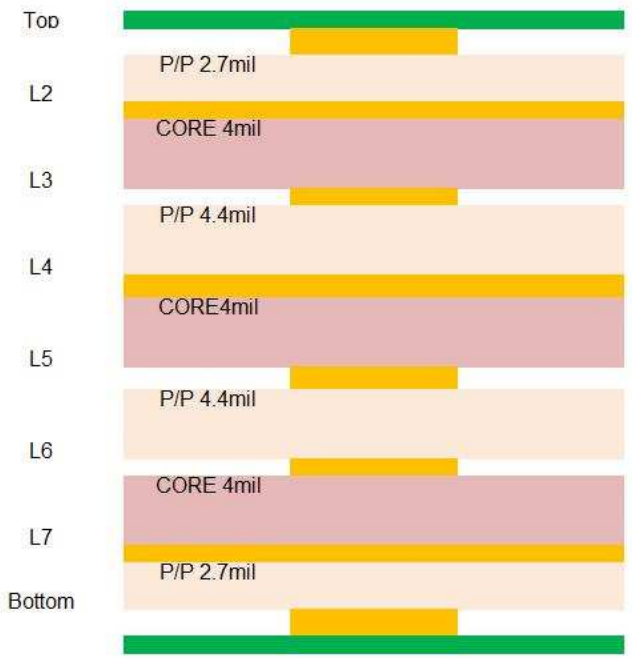
CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIGNAL	VOLTAGE	G3	S5	S3	S0
RTC	3.3V	O	O	O	O
PVBAT	12V	X	O	O	O
P3V3DS	3.3V	X	O	O	O
P3V3A	3.3V	X	O	O	O
P3V3S	3.3V	X	X	X	O
P5V0DS	5V	X	O	O	O
P5V0A_USB	5V	X	O	O	O
P5V0S	5V	X	X	X	O
P1V05A	1.05V	X	O	O	O
P1V2	1.2V	X	X	O	O
P2V5	3.3V	X	X	O	O
P1V8DS	1.8V	X	O	O	O
P1V5S	1.5V	X	X	X	O
PVCCIO	0.95V	X	X	X	O
PVCC_PRIM	1.05V	X	O	O	O
PVCORE	SVID	X	X	X	O
PVCCGT	SVID	X	X	X	O
PVCCSA	1V	X	X	X	O
PVCCSFR	1.05V	X	X	O	O
PVCORE_DGPU	SVID	X	X	X	O
P1V35S_DGPU	1.35V	X	X	X	O
PVDDCI_DGPU	SVID	X	X	X	O
P1V8S_DGPU	1.8V	X	X	X	O

STACK_UP for 8 layer-0.9mm-5Signal



0.60mil	(Solder Mask)	1 OZ min
1.55mil	(Hoz + Plating)	
2.70mil		
0.60mil	(GND)	H OZ
4.00mil		
0.60mil	(SIGNAL)	H OZ
4.40mil		
1.30mil	(VCC)	1 OZ
4.00mil		
1.30mil	(SIGNAL)	1 OZ
4.40mil		
0.60mil	(SIGNAL)	H OZ
4.00mil		
0.60mil	(GND)	H OZ
2.70mil		
1.55mil	(Hoz + Plating)	1 OZ min
0.60mil	(Solder Mask)	

ideal: 35.50mil
0.90mm

Premium-U Port	Base-U Port	Oleander 13" x360/Camellia 13/14" Base-U
USB30_P1/PCIe1	USB30_P1	USB Type A(Left)
USB30_P2/PCIe2	USB30_P2	USB Type A(Left)
USB30_P3/PCIe3	USB30_P3	Free
USB30_P4/PCIe4	USB30_P4	Free
USB30_P5/PCIe5	PCIe5	TBT
USB30_P6/PCIe6	PCIe6	TBT
PCIe7(GbE)	PCIe7(GbE)	TBT
PCIe8(GbE)	PCIe8(GbE)	TBT
PCIe9 (GbE)	PCIe9 (GbE)	SSD(NVMe)
PCIe10	PCIe10	SSD(NVMe)
PCIe11 /SATA 0	PCIe11 /SATA 0	SSD(NVMe)
PCIe12 /SATA 1A	PCIe12 /SATA 1A	SSD(NVMe)/SATA SSD
PCIe13 (GbE)	PCIe13 (GbE)	Free
PCIe14 (GbE)	PCIe14 (GbE)	WLAN
PCIe15 /SATA 1B	PCIe11	Free
PCIe16 /SATA 2	PCIe12	WWAN(PCIE)

DDI		Premium-U Port	Base-U Port	
0-eDP		DDI PortA	DDI PortA	eDP
1		DDI PortB	DDI PortB	Demux to TR DDI2/HDMI
2		DDI PortC	DDI PortC	TR DDI1
USB2				
1		USB 2.0 #1	USB 2.0 #1	USB Type A(Right)
2		USB 2.0 #2	USB 2.0 #2	Camera
3		USB 2.0 #3	USB 2.0 #3	Smart Card
4		USB 2.0 #4	USB 2.0 #4	USB Type A(Left)
5		USB 2.0 #5	USB 2.0 #5	Type C2
6		USB 2.0 #6	USB 2.0 #6	Type C1
7		USB 2.0 #7	USB 2.0 #7	Finger Print Reader
8		USB 2.0 #8	NA	
9		USB 2.0 #9	NA	WWAN (USB2.0)
10		USB 2.0 #10 (CNVI enable platform, this port need to for BT port)	USB 2.0 #10 (CNVI enable platform, this port need to for BT port)	Bluetooth

		PCH GPIO			
		BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4
		GPP_H12	GPP_H13	GPP_H14	GPP_H15
CPU Socket Board / Reserved	0	0	0	0	0
FIP board / Reserved	1	0	0	0	1
DB1	2	0	0	1	0
SI1	3	0	0	1	1
SI1R	4	0	1	0	0
	5	0	1	0	1
SI2	6	0	1	1	0
SI2R	7	0	1	1	1
	8	1	0	0	0
SI3	9	1	0	0	1
	10	1	0	1	0
PV	11	1	0	1	1
PVR	12	1	1	0	0
	13	1	1	0	1
MV	14	1	1	1	0
	15	1	1	1	1

	BIOS Group 2			
	PCH PLT_ID			
	0: P(CMIT) ; 1 : W(mWS)	0:14" ; 1:15"	BIOS Group 2	SG_IN ; UMA-0 ; DSC -1
	PLT_ID2	PLT_ID3	PLT_ID4	SG_IN
	GPP_F9	GPP_F10	GPP_A16	GPP_F3
Camellia 15W UMA	1	1	1	0
Camellia 15W DSC	1	1	1	1
Camellia 15P UMA	0	1	1	0
Camellia 15P DSC	0	1	1	1
Camellia 14W DSC	1	0	1	1

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
DESIGN INFORMATION

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-D-D	X01

CHANGE SI	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

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