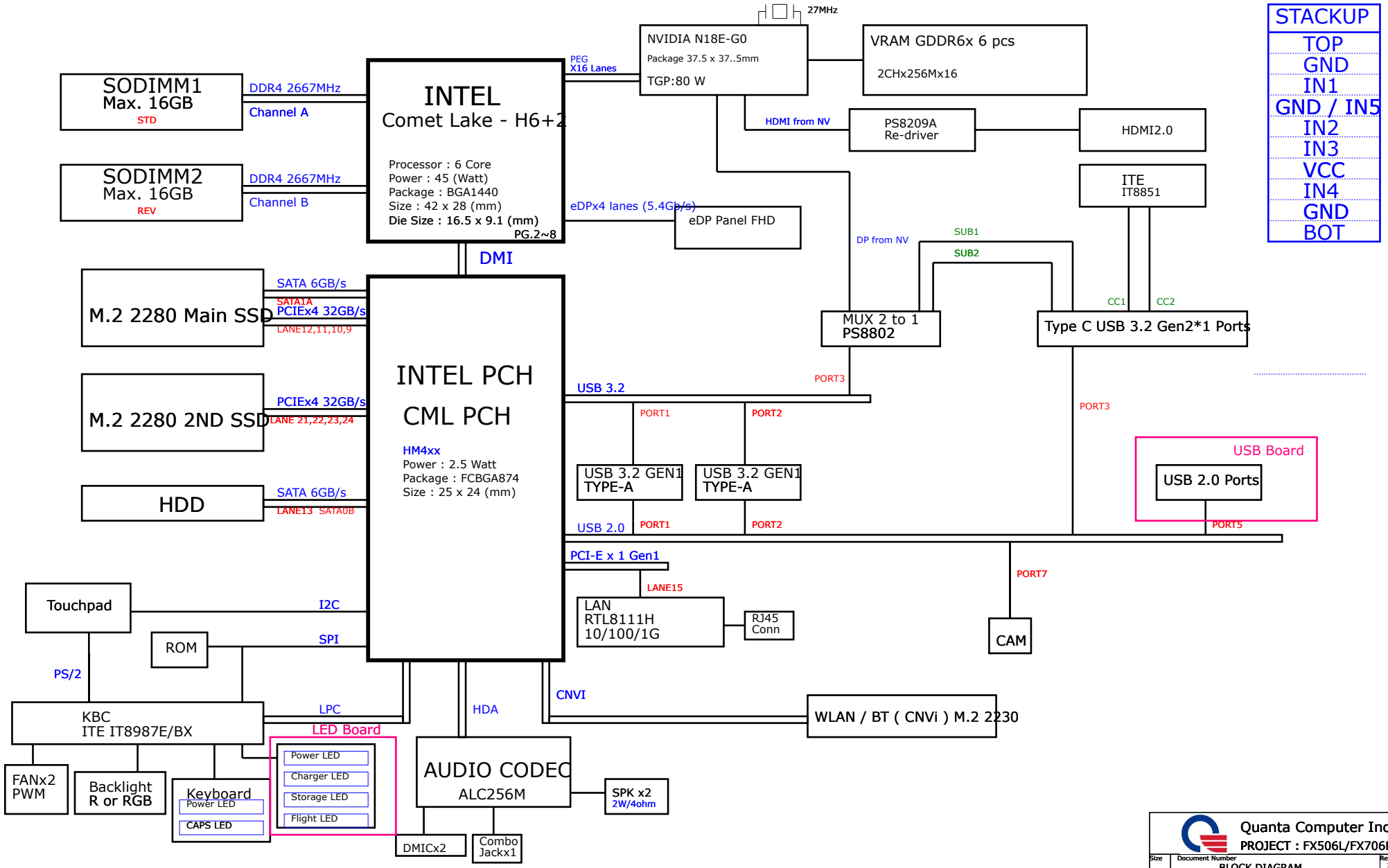
ASUS FX506LU N18E-G0 Block Diagram

01



STACKUP
TOP
GND
IN1
GND / IN5
IN2
IN3
VCC
IN4
GND
BOT

Quanta Computer Inc.
PROJECT : FX506L/FX706L

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	BLOCK DIAGRAM	1A

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Model
FX506LU

REV
ER

CHANGE LIST

Item	Stage	Page	Owner	Change explanation
01	ER	29	EE	ER-000:Del RUN_ON for 1.2V_MUX enable....1113
02	ER	29	EE	ER-001:Change G9090 to G966I to solve PD issue.and +1.2V_HDMI ripple issue....1113
03	ER	29	EE	ER-002:Add N-MOSFET to +1.2V_HDMI for ripple issue....1113
04	ER	39	EE	ER-004:Change +1.2V to +1.2V_HDMI power rail name....1113
05	ER	29	EE	ER-005:Del +3V power rail and SR9 and SR7 to shortpad....1113.
06	ER	29	EE	ER-006:Change +3V_PD to LDO for ripple issue....1113.
07	ER	39	EE	ER-007:ADD DISCHARGE FOR to +1.2V_HDMI power rail name....1113
08	ER	29	EE	ER-008:No mount SR82 for surge issue....1113.
09	ER	29	EE	ER-009:DEL PD to MUX SMBUS....1113.
10	ER	29	EE	ER-010:Change no mount:SQ1,SR66,SR67, NO USED....1113.
11	ER	39	EE	ER-011:Change no mount:HQ3, NO USED....1113.
12	ER	29	EE	ER-012:Change SR61,SR62,SR63 TO NO-MOUNT for shortpad....1113.
13	ER	11	EE	ER-013:Change R206 TO NO-MOUNT for shortpad....1113.
14	ER	16	EE	ER-014:Change R858 and C1094,R856 TO NO-MOUNT....1113.
15	ER	7	EE	ER-015:Change C269 1000P to 10U_4 for power ripple....1113.
16	ER	18	EE	ER-016:Add 0.1U near MR5....1113.
17	ER	19	EE	ER-017:Add 0.1U near MR10....1113.
18	ER	32	EE	ER-018:Change C1116 *47U to 10U_4 for ripple....1113.
19	ER	22	EE	ER-019:Change GPIO27_IFPC_HPD to GPIO27_IFPC_HPD# for Low active....1113.
20	ER	22	EE	ER-020:Change GPIO18_IFPE_HPD to GPIO18_IFPE_HPD# for Low active....1113.
21	ER	28	EE	ER-021:Del RP1/RP2/RP3/RP4 and EMI by pass for EMI request....1113.
22	ER	07	EE	ER-022:Change C289,C73,C72 from 47uF to 22uF for PASs VR1T...1119
23	ER	29	EE	ER-023:Change SU10 part number for E ver and 08FW to fix PD2.0 fail issue....1120.
24	ER	36	EE	ER-024:Change KR122 00hm to no-mount for no support....1120
25	ER	28	EE	ER-025:Change AR47,AR48 to BLM15AG221SN1D and C1072 C1073 to 10P For EMI issue and signal pass....1122.
26	ER	31	EE	ER-026: Change 2.1ohm to 5.1ohm for fix TDR issue....1122.
27	ER	12	EE	ER-027: Change R43 to no-mount and add R874 100K to GND for fixed GPU timing issue....1122.
28	ER	23	EE	ER-028: Change VR113 to 10Kfor fixed GPU timing issue....1122.
29	ER	34	EE	ER-029: Change C355,C356 to no-mount for fix TP timing issue....1122.
30	ER	35	EE	ER-030:Add AR47 moat resistor between AGND&DGND and connect to AU1 pin20 for active speaker noise issue in S5....1122.
31	ER	37	EE	ER-031:Del KQ15/KQ13 for no support Red backlight....1125.
32	ER	23	EE	ER-032:Fix voltage ripple over spec ....1128.
33	ER	35	EE	ER-031:AR14 and AR5 change from 22 ohm to 10 ohm increasing the FSOV margin.
34	ER	30	EE	ER-032:Remove CON6 for USB board FFC CONN
35	ER	30	EE	ER-E33:Reserve CON6 for USB board FFC CONN.....1206
36	ER	31	EE	ER-E34:KR64, KR65, KR66, KR67, KR68 change from 390 to 931 ohm for brigtness
37	ER			
38	ER			
39	ER	54	Power	ER-001:PR631 from 1000hm to 1050hm for +1.0V_GPU output voltage.
40	ER	48	Power	ER-002:Add PC169 & PC170 47pF for ASUS SDW.
41	ER	41	Power	ER-003:Change PR1093 from 16.9k to 18.7k to set IA iccmax 128A for CML H base.
42	ER	41	Power	ER-004:Change PC1061 from 68pF to 330pF to correct L_DCR matching.
43	ER	41	Power	ER-005:Change PR1078 from 422 to 442 ohm to to set OCP 180A for H62.
44	ER	41	Power	ER-006:Change PC1068 from NI to 47nF to correct L_CDR matching.
45	ER	41	Power	ER-008:Change PR1078 from 365 to 287 ohm to set OCP 116A for H42.
46	ER	41	Power	ER-009:Change PR1057 to 71.2k to correct IMONA for H42.
47	ER	41	Power	ER-010:Change PR1070 from 5.11k to 3.3k to correct DCLL for H42.
48	ER	43	Power	ER-011:PC1333,PC1334,PC1335,PC1336,PC1337,PC1338 add 22uF to reduce ripple by VTT test
49	ER	41	Power	ER-012:Change PC1044 from 10nF to 15nF to correct L_DCR matching for SA.
50	ER	41	Power	ER-013:Change PC1050 from 220pF to 680pF to reduce undershoot for SA.
51	ER	47	Power	ER-014:Delete PD12 & PD13 for SHDN# issue.
52	ER	47	Power	ER-015:PC157 1000P change to 2200P for meet HDD rise time SPEC.
53	ER	47	Power	ER-016:PC164 1000P change to 680P for meet TP rise time SPEC.
54	ER	45	Power	ER-017:PR1397 change to 6.49K+-1% for output voltage up.
55	ER	54	Power	ER-018:PR642 change from 24.9K to 25.5K by EE request
56	ER	56	Power	ER-019: PC295 & PC299 NC, 180W/G0 just 9pcs
57	ER	41-56	Power	ER-020:0ohm change to short pad.
58	ER	41-56	Power	ER-021:Remove output short pad.
59	ER	47	Power	ER-022:Reserve MAIND signal
60	ER	45	Power	ER-023: +1.05V_VCCSTG enable signal change to RUN_ON by EE request
61	ER	47~49	Power	ER-024:add test point PTP1~6 for ASUS request
62	ER	47	Power	ER-025:Reserve PC1405 for EMI request
63	ER	50	Power	ER-026:PU24 change to MP2886AGU-0144-Z by nVidia requests VRM from RC mode to liner mode
64	ER	49	Power	ER-027:Set Pmon(max) on 360W
65	ER	53	Power	ER-028:Fix FBVDDQ voltage due to support G0 only
66	ER	44	Power	ER-029:VCCIO enable signal change to CI0_GATE# by EE request
67	ER	45	Power	ER-030: +1.05V_VCCSTG enable signal change to CI0_VCCSTG_EN; mount PU1332 for debug

DOC NO.	PROJECT MODEL :	BKLG/BKLH	APPROVED BY:		DATE:	2018/01/17
	PART NUMBER:		DRAWING BY:		REVISON:	1A

02

Quanta Computer Inc.
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	POWER UP SEQUENCE	2A

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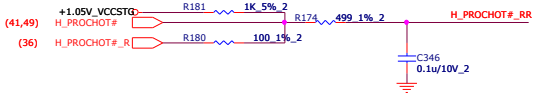
Comet Lake Processor (CLK,MISC,JTAG)

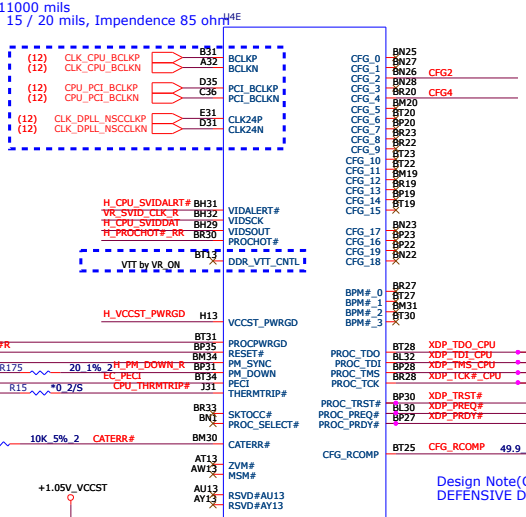
03

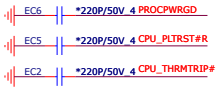
Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm

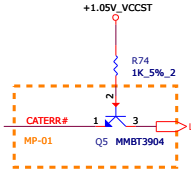
PROCHOT# (50ohm)
Trace Length <11 inches

Cb need placment near VR







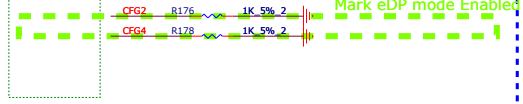


Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

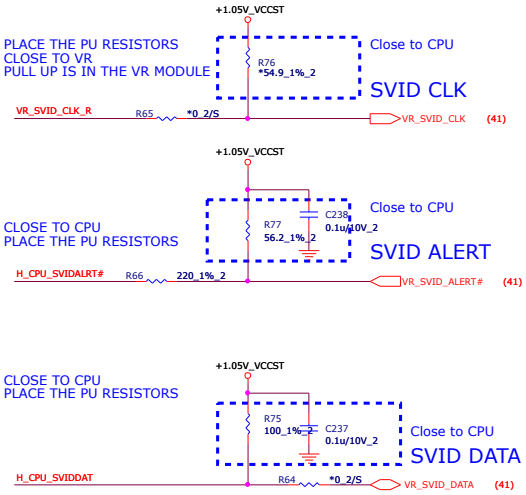
0 Enable; SET DFX ENABLED BIT IN DEBUG
1 , Disable;



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OxM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	

CPU CORE SVID

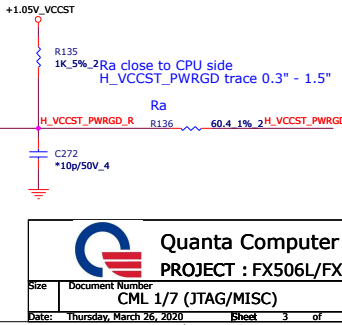
Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.



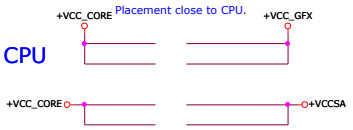
H_VCCST_PWRGD
C270 *0.1U/10V/X5R_2

CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A



Under CPU



11/21 updated FP

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	CML 1/7 (JTAG/MISC)	2A
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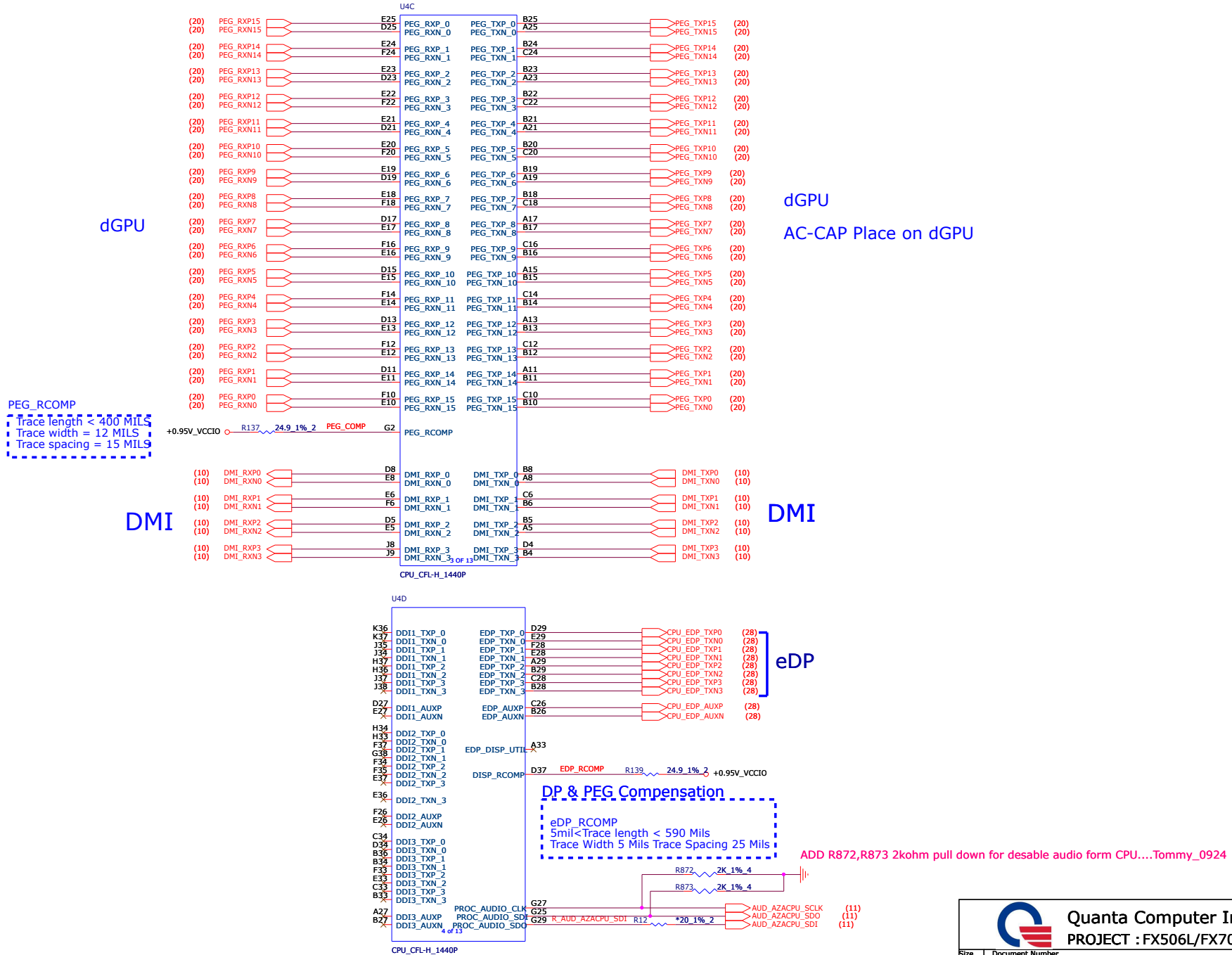
Comet Lake Processor (DMI,PEG,FDI)



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	CML 2/7 (DMI/EDP/PEG)	2A
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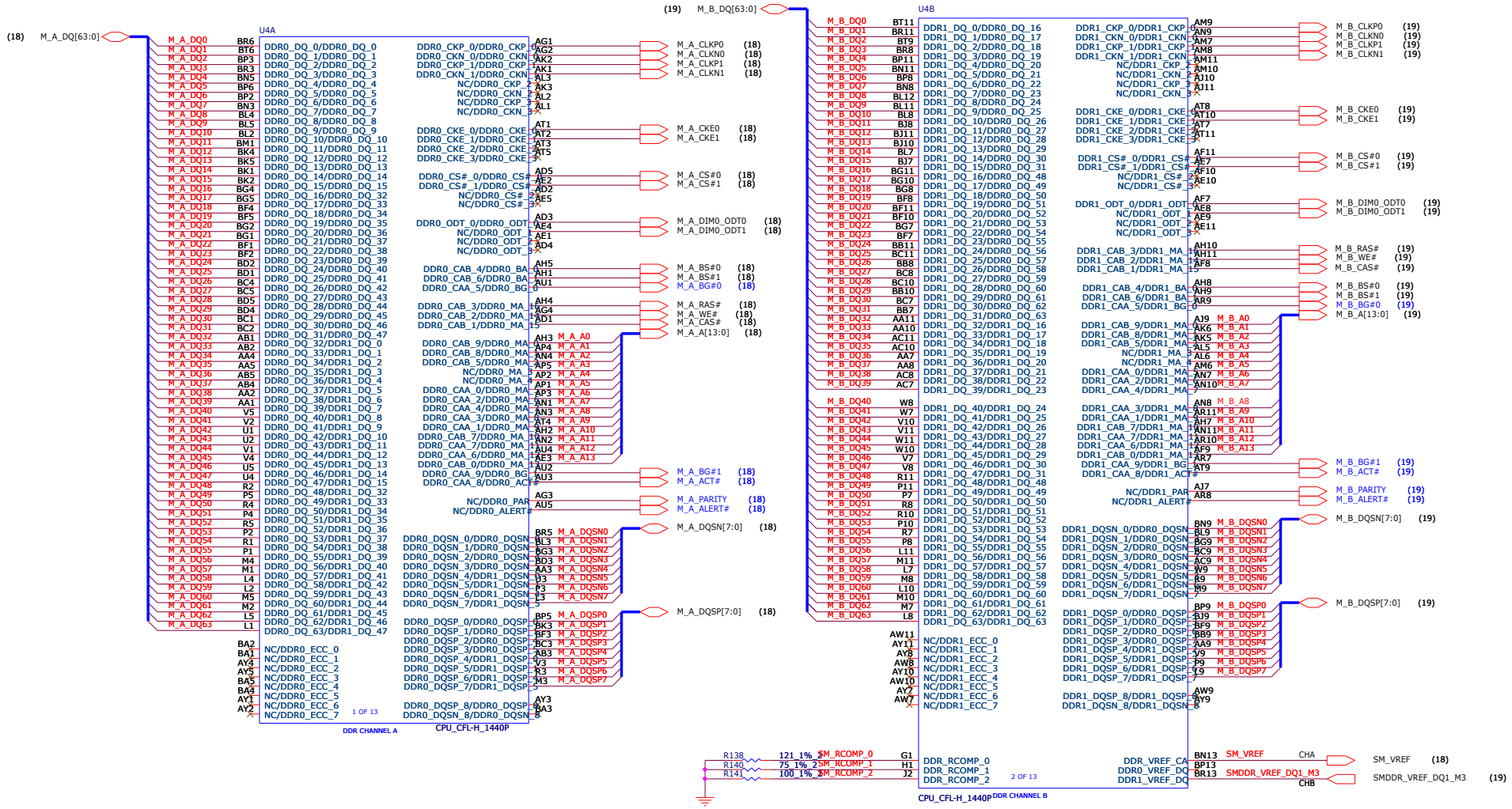
Comet Lake Processor (DDR4)

Interleaved

05



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