Cyborg 16H Schematic

Intel TGL-H DVT

2020/10/06

REV : X01

DY : None Installed
DIS: DISCRTE OPTIMUS installed

TGL-H

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Title: *Cover Page*

Size	Document Number	Rev
A4	Cyborg_TGL-H RTX	X01

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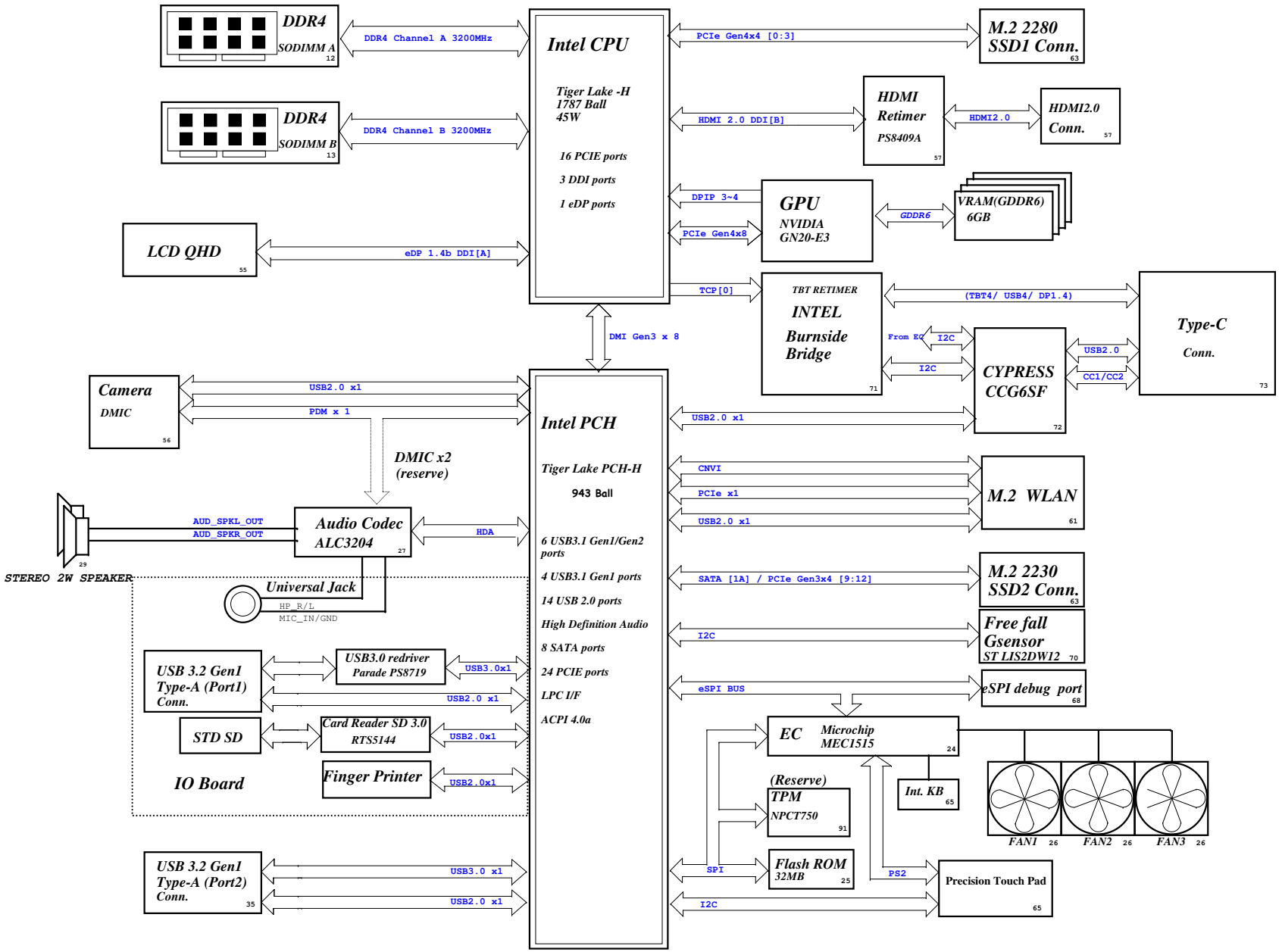
Project Code : QRQY00000944
PCB P/N : 19843-SA
Revision : X00

Cyborg TGL-H RTX Block Diagram



CHARGER		
ISL9538		44
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	

SYSTEM DC/DC		
SY8288CRAC-GP TPS51393PRJER-GP		45
INPUTS	OUTPUTS	
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5	

CPU Core Power		
NCP81307MNTXG-GP NCP302045MNTWG*4 RT6543AGQW-GP		46~50
INPUTS	OUTPUTS	
DCBATOUT DCBATOUT DCBATOUT DCBATOUT	VCC_CORE +VCCGT +VCCGT (23e) +VCCSA	

DDR4 SUS		
TPS51486RJER-GP		51
INPUTS	OUTPUTS	
DCBATOUT 3D3V_S5	1D2V_S3 0D6V_S0 2D5V_S3	

CPU VCCPRIM_CORE 1V		
		11
INPUTS	OUTPUTS	
1D0V_S5	+VCCPRIM_CORE	

CPU DCDC-V1D00A		
AOZ2262QI-10-GP-U		53
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	

LDO-V1D8V		
APL5934KAI-TRG-GP-U		54
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	

5V/3V S0		
G2898KD1U-GP		40
INPUTS	OUTPUTS	
5V_S5 3D3V_S5	5V_S0 3D3V_S0	

1D8V_AON_S0		
G2898KD1U-GP		86
INPUTS	OUTPUTS	
3D3V_S0	1D8V_AON_S0	

1V_VGACORE_S0		
MP2884AGU-0916-GP		85
INPUTS	OUTPUTS	
DCBATOUT	1V_VGACORE_S0	

1V_VGA_S0		
TPS51396RJER-GP		86
INPUTS	OUTPUTS	
DCBATOUT	1V_VGA_S0	

1D35V_VGA_S0		
RT8816BGQW-GP		86
INPUTS	OUTPUTS	
DCBATOUT	1D35V_VGA_S0	

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Title: Block Diagram

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Custom	Cyborg_TGL-H RTX	X01

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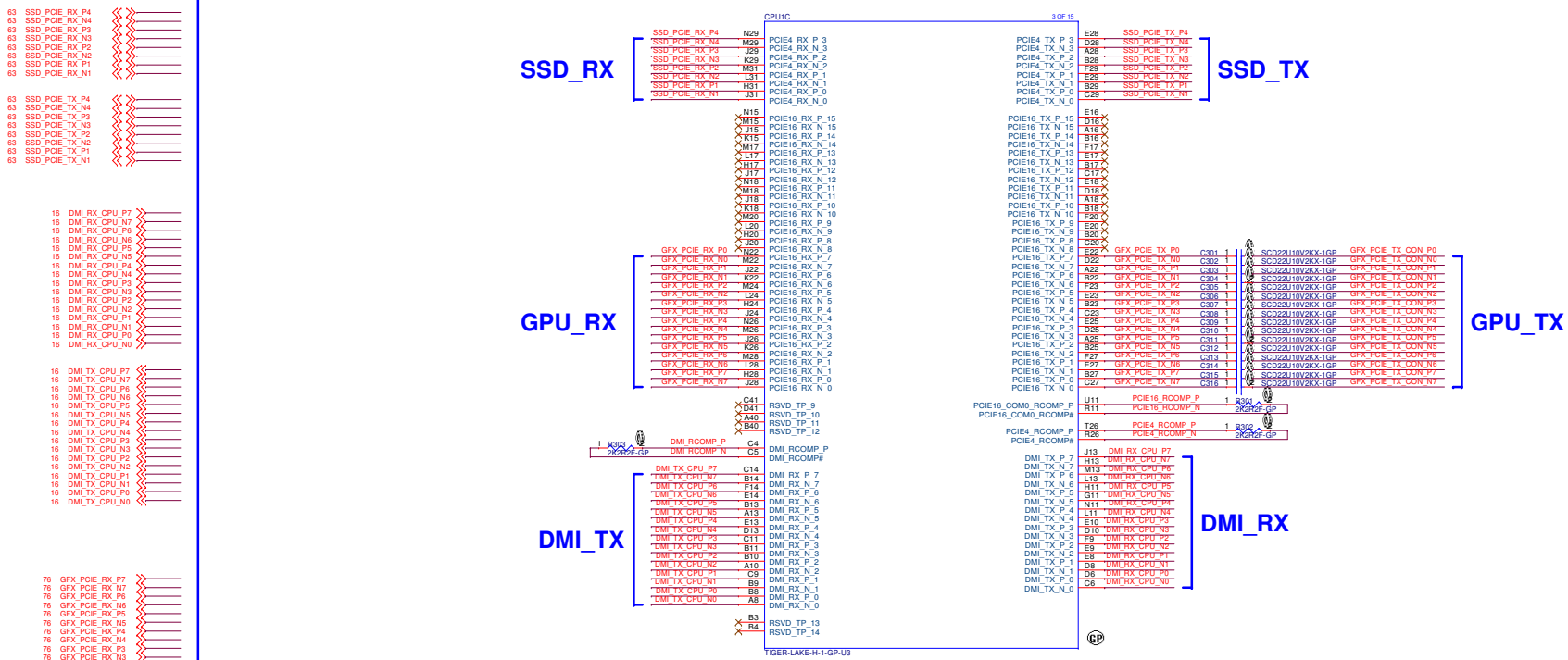

575683_TGL_EDS_Vol1_Rev1p0 P.108

Table 7-2. PCI Express* 16-lane Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes															
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
PCIe Controller							GPU PCIe 011								PCIe 010							
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
PCIe Controller							PCIe 010								PCIe 011				PCIe 012			
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
PCIe Controller							PCIe 012				PCIe 011				PCIe 010							
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

618429_TGL_H_PDG_Rev1p0 RCOMP

Pin Name	PCIE4_RCOMP_P PCIE4_RCOMP_N	PCIE16_COM0_RCOMP_P PCIE16_COM0_RCOMP_N	DMI_RCOMP_P DMI_RCOMP_N
Board Rterm (ohm)	2.2KΩ±1% Differential	2.2KΩ±1% Differential	2.2KΩ±1% Differential
Board Rdc (ohm)	<0.5 sum both traces	<0.5 sum both traces	<0.5 sum both traces
Board Cap (pF)	2	2	N/A
Spacing for Breakout (um)	MS: 500 SL/DSL: 380	MS: 500 SL/DSL: 380	MS: 500 SL/DSL: 380
Spacing for Mainroute (um)			
DDR			
HDMI			
DP			
eDP			
DSI			
CSI			
Type-C			
PCIe4 x4	X		
PCIe4 x16		X	
DMI			X
DPIP[0/1/2/3]			
ModPHY			
USB2			
GPIO_1.8V/3.3V			
SoundWire			
GPIO_1.8V			
XTAL			
CNVI_DPHY			

Dell_CY21_CSB_HSIO_Port_Assignment_Rev0.1_2020-04-07_Cyborg-H

Ball	HSIO Lane	HSIO Type and Lane	CY21 Port Mapping	Cyborg-H
EN38	0	USB-C 0 (DDI TCP0; USB3 support up to SuperSpeed; DP up to HBR3, HDMI up to 5.94)	TBT #0	TBT #0
I31	4	PCIe 4.0 #0	PCIe x 4 <Gen4> (NVMe storage)	CPU M.2 SSD <Gen4> (PCIex4)
L31	5	PCIe 4.0 #1		PCIe x 4 <Gen4> (NVMe storage)
K29	6	PCIe 4.0 #3		
M29	7	PCIe 4.0 #4		
J28	4	PCIe 16 #0	PCIe x 16	dGPU (x8)
L28	5	PCIe 16 #1		
K26	6	PCIe 16 #2		
M26	7	PCIe 16 #3		
J24	4	PCIe 16 #4		dGPU (x8)
L24	5	PCIe 16 #5		
K22	6	PCIe 16 #6		
M22	7	PCIe 16 #7		

Ball	PCH HSIO Lane	HSIO Type and Lane	CY21 Port Mapping	Cyborg-H
L24	14	DMI 7	DMI	DMI x 8
P22	15	DMI 6		
R26	16	DMI 5		
H26	17	DMI 4		
J26	18	DMI 3		
L29	19	DMI 2		
H30	20	DMI 1		
L31	21	DMI 0		

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Title: CPU (PEG/DMI/PCIE4.0)

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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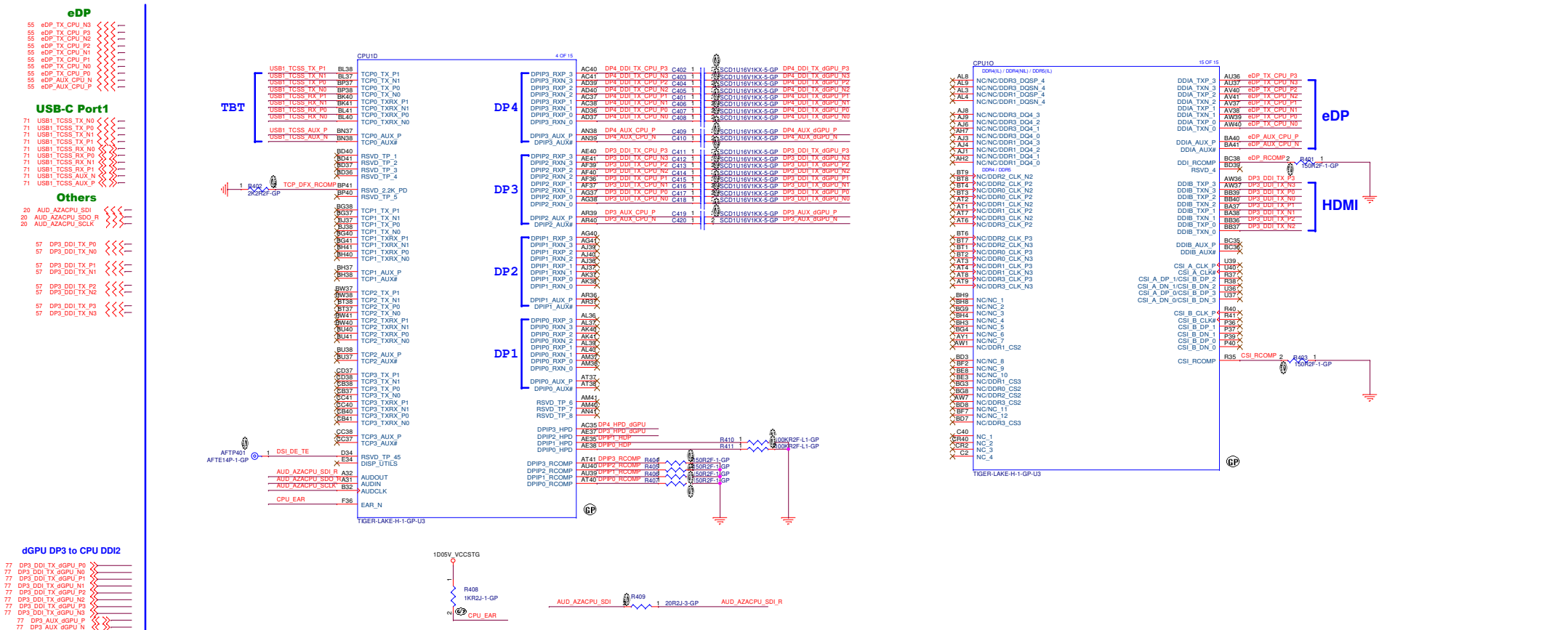
eDP
55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
USB-C Port1
71 USB1_TCSS_TX_N0
71 USB1_TCSS_TX_P0
71 USB1_TCSS_TX_N1
71 USB1_TCSS_TX_P1
71 USB1_TCSS_RX_N0
71 USB1_TCSS_RX_P0
71 USB1_TCSS_RX_N1
71 USB1_TCSS_RX_P1
71 USB1_TCSS_AUX_N
71 USB1_TCSS_AUX_P
Others
20 AUD_AZACPU_SDI
20 AUD_AZACPU_SDO_R
20 AUD_AZACPU_SCLK
57 DP3_DDI_TX_P0
57 DP3_DDI_TX_N0
57 DP3_DDI_TX_P1
57 DP3_DDI_TX_N1
57 DP3_DDI_TX_P2
57 DP3_DDI_TX_N2
57 DP3_DDI_TX_P3
57 DP3_DDI_TX_N3
dGPU DP3 to CPU DDI2
77 DP3_DDI_TX_dGPU_P0
77 DP3_DDI_TX_dGPU_N0
77 DP3_DDI_TX_dGPU_P1
77 DP3_DDI_TX_dGPU_N1
77 DP3_DDI_TX_dGPU_P2
77 DP3_DDI_TX_dGPU_N2
77 DP3_DDI_TX_dGPU_P3
77 DP3_DDI_TX_dGPU_N3
77 DP3_AUX_dGPU_P
77 DP3_AUX_dGPU_N
79 DP3_HPD_dGPU
dGPU DP4 to CPU DDI3
77 DP4_DDI_TX_dGPU_P0
77 DP4_DDI_TX_dGPU_N0
77 DP4_DDI_TX_dGPU_P1
77 DP4_DDI_TX_dGPU_N1
77 DP4_DDI_TX_dGPU_P2
77 DP4_DDI_TX_dGPU_N2
77 DP4_DDI_TX_dGPU_P3
77 DP4_DDI_TX_dGPU_N3
77 DP4_AUX_dGPU_P
77 DP4_AUX_dGPU_N
79 DP4_HPD_dGPU
CPU1D
4 OF 15
TBT
DP4
DP3
DP2
DP1
TCP0_TX_P1
TCP0_TX_N1
TCP0_TX_P0
TCP0_TX_N0
TCP0_TXRX_P1
TCP0_TXRX_N1
TCP0_TXRX_P0
TCP0_TXRX_N0
TCP0_AUX_P
TCP0_AUX#
RSVD_TP_1
RSVD_TP_2
RSVD_TP_3
RSVD_TP_4
RSVD_2.2K_PD
RSVD_TP_5
TCP1_TX_P1
TCP1_TX_N1
TCP1_TX_P0
TCP1_TX_N0
TCP1_TXRX_P1
TCP1_TXRX_N1
TCP1_TXRX_P0
TCP1_TXRX_N0
TCP1_AUX_P
TCP1_AUX#
TCP2_TX_P1
TCP2_TX_N1
TCP2_TX_P0
TCP2_TX_N0
TCP2_TXRX_P1
TCP2_TXRX_N1
TCP2_TXRX_P0
TCP2_TXRX_N0
TCP2_AUX_P
TCP2_AUX#
TCP3_TX_P1
TCP3_TX_N1
TCP3_TX_P0
TCP3_TX_N0
TCP3_TXRX_P1
TCP3_TXRX_N1
TCP3_TXRX_P0
TCP3_TXRX_N0
TCP3_AUX_P
TCP3_AUX#
RSVD_TP_45
DISP_UTILS
AUDOUT
AUDIN
AUDCLK
EAR_N
TIGER-LAKE-H-1-GP-U3
TCP_DFX_RCOMP
DSI_DE_TE
AUD_AZACPU_SDI_R
AUD_AZACPU_SDO_R
AUD_AZACPU_SCLK
CPU_EAR
DP4_DDI_TX_CPU_P3
DP4_DDI_TX_CPU_N3
DP4_DDI_TX_CPU_P2
DP4_DDI_TX_CPU_N2
DP4_DDI_TX_CPU_P1
DP4_DDI_TX_CPU_N1
DP4_DDI_TX_CPU_P0
DP4_DDI_TX_CPU_N0
DP4_AUX_CPU_P
DP4_AUX_CPU_N
DP3_DDI_TX_CPU_P3
DP3_DDI_TX_CPU_N3
DP3_DDI_TX_CPU_P2
DP3_DDI_TX_CPU_N2
DP3_DDI_TX_CPU_P1
DP3_DDI_TX_CPU_N1
DP3_DDI_TX_CPU_P0
DP3_DDI_TX_CPU_N0
DP3_AUX_CPU_P
DP3_AUX_CPU_N
DP4_DDI_TX_dGPU_P3
DP4_DDI_TX_dGPU_N3
DP4_DDI_TX_dGPU_P2
DP4_DDI_TX_dGPU_N2
DP4_DDI_TX_dGPU_P1
DP4_DDI_TX_dGPU_N1
DP4_DDI_TX_dGPU_P0
DP4_DDI_TX_dGPU_N0
DP4_AUX_dGPU_P
DP4_AUX_dGPU_N
DP3_DDI_TX_dGPU_P3
DP3_DDI_TX_dGPU_N3
DP3_DDI_TX_dGPU_P2
DP3_DDI_TX_dGPU_N2
DP3_DDI_TX_dGPU_P1
DP3_DDI_TX_dGPU_N1
DP3_DDI_TX_dGPU_P0
DP3_DDI_TX_dGPU_N0
DP3_AUX_dGPU_P
DP3_AUX_dGPU_N
DP4_HPD_dGPU
DP3_HPD_dGPU
DP3_RCOMP
DP2_RCOMP
DP1_RCOMP
DP0_RCOMP
R404 150R2F-1-GP
R405 150R2F-1-GP
R406 150R2F-1-GP
R407 150R2F-1-GP
R410 100KR2F-1-GP
R411 100KR2F-1-GP
AFTP401 AFTE14P-1-GP
R408 1KR2J-1-GP
R409 20R2J-3-GP
1D05V_VCCSTG
CPU_EAR
AUD_AZACPU_SDI
AUD_AZACPU_SDI_R
CPU1O
15 OF 15
DDR4(LL) / DDR4(NLL) / DDR5(LL)
DDR4 / DDR5
eDP
HDMI
DDIA_TXP_3
DDIA_TXN_3
DDIA_TXP_2
DDIA_TXN_2
DDIA_TXP_1
DDIA_TXN_1
DDIA_TXP_0
DDIA_TXN_0
DDIA_AUX_P
DDIA_AUX#
DDI_RCOMP
RSVD_4
DDIB_TXP_3
DDIB_TXN_3
DDIB_TXP_2
DDIB_TXN_2
DDIB_TXP_1
DDIB_TXN_1
DDIB_TXP_0
DDIB_TXN_0
DDIB_AUX_P
DDIB_AUX#
CSI_A_CLK_P
CSI_A_CLK#
CSI_A_DP_1/CSI_B_DP_2
CSI_A_DN_1/CSI_B_DN_2
CSI_A_DP_0/CSI_B_DP_3
CSI_A_DN_0/CSI_B_DN_3
CSI_B_CLK_P
CSI_B_CLK#
CSI_B_DP_1
CSI_B_DN_1
CSI_B_DP_0
CSI_B_DN_0
CSI_RCOMP
R491 150R2F-1-GP
R493 150R2F-1-GP
TIGER-LAKE-H-1-GP-U3
618429_TGL_H_PDG_Rev1p0 P.136
Table 64. CFG Signals Functionality and Termination
CFG
Description
Termination
Resistor
EAR
Stall CPU reset sequence until de-asserted:
Pull-up to VCCSTG
1K ohm
continued...
- 1 = (Default) Normal Operation; No stall.
- 0 = Stall
618697_TGL_H_DDR4_SCH_REV1P1 P.13
R4D47 20 5% CHIP 1/16W 0402 A93549-030
DP_UTIL
AUD_AZACPU_SDI_R
AUD_AZACPU_SDO_R
AUD_AZACPU_SCLK
CPU_EAR
AUD_AZACPU_SDI
RSVD_TP_45
DISP_UTILS
AUDOUT
AUDIN
AUDCLK
EAR_N
LPID7081
618429_TGL_H_PDG_Rev1p0 RCOMP
Pin Name
DDI_RCOMP
CSI_RCOMP
TC_RCOMP_P TC_RCOMP_N
TCP0_MBIAS_RCOMP_P
DPIP[0/1/2/3]_RCOMP
Board Rterm (ohm)
150Ω±1% to GND
150Ω±1% to GND
150Ω±1% Differential
2.2kΩ±1% to GND
150Ω±1% to GND
Board Rdc (ohm)
<0.2
<0.5
<0.5 sum both traces
<0.5
<0.5
Board Cap (pF)
N/A
N/A
N/A
2
N/A
Spacing for Breakout (um)
MS: 500 SL/DSL: 380
MS: 500 SL/DSL: 380
MS: 500 SL/DSL: 380
MS: 500 SL/DSL: 380
MS: 500 SL/DSL: 380
Spacing for Mainroute (um)
DDR
HDMI
DP
eDP
DSI
CSI
Type-C
PCIe4 x4
PCIe4 x16
DMI
DPIP[0/1/2/3]
ModPHY
USB2
GPIO_1.8V/3.3V
SoundWire
GPIO_1.8V
XTAL
CNVi_DPHY
575683_TGL_EDS_Vol1_Rev1p0 P.115
Table 9-1. Display Ports Availability and Link Rate for UP4/UP3/H-Processor Lines
Port
UP4-Processor Line
UP3-Processor Line
H-Processor Line
DDI A[1,2]
eDP* up to HBR3 MIPI DSI up to 2.5 Gbps
eDP* up to HBR3 MIPI DSI up to 2.5 Gbps[5]
eDP* up to HBR3
DDI B[2]
eDP* up to HBR3 DP* up to HBR2 HDMI* up to 5.94 Gbps MIPI DSI up to 2.5 Gbps
eDP* up to HBR3 DP* up to HBR2 HDMI* up to 5.94 Gbps
eDP* up to HBR3 DP* up to HBR2 HDMI* up to 5.94 Gbps
DDI TCP0[3]
DP* up to HBR3 HDMI* up to 5.94 Gbps
DP* up to HBR3 HDMI* up to 5.94 Gbps
DP* up to HBR3 HDMI* up to 5.94 Gbps
DDI TCP1[3]
DP* up to HBR3 HDMI* up to 5.94 Gbps
DP* up to HBR3 HDMI* up to 5.94 Gbps
DP* up to HBR3 HDMI* up to 5.94 Gbps
DDI TCP2[3]
DP* up to HBR3 HDMI* up to 5.94 Gbps
DP* up to HBR3 HDMI* up to 5.94 Gbps
DP* up to HBR3 HDMI* up to 5.94 Gbps
DDI TCP3[3]
N/A
DP* up to HBR3 HDMI* up to 5.94 Gbps
DP* up to HBR3 HDMI* up to 5.94 Gbps
DPIP0[4]
N/A
N/A
DP* up to HBR3
DPIP1[4]
DP* up to HBR3
DPIP2[4]
DP* up to HBR3
DPIP3[4]
DP* up to HBR3
Dell_CY21_CSB_HSIO_Port_Assignment_Rev0.1_2020-04-07_Cyborg-H
Ba
HSIO La
HSIO Type and Lane
CY21 Port Mapping
Cyborg-H
USB-C 0
DDI TCP0
USB3 support up to SuperSpeed
DP up to HBR3, HDMI up to 5.94
BN38
0
BA41
BC36
AT38
AR37
AR40
AN39
Display Interfaces
DDI A
DDI B
DPIP0
DPIP1
DPIP2
DPIP3
eDP up to HBR3
MIPI_1 up to 2.5 Gbps
HDMI up to HBR3
DP up to HBR3
TBT #0
eDP
HDMI2.0
DPIN0
DPIN1
DPIN2
DPIN3
TGL-H
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Title
CPU (DDI/EDP/TCP/DP/CSI)
Size A2
Document Number
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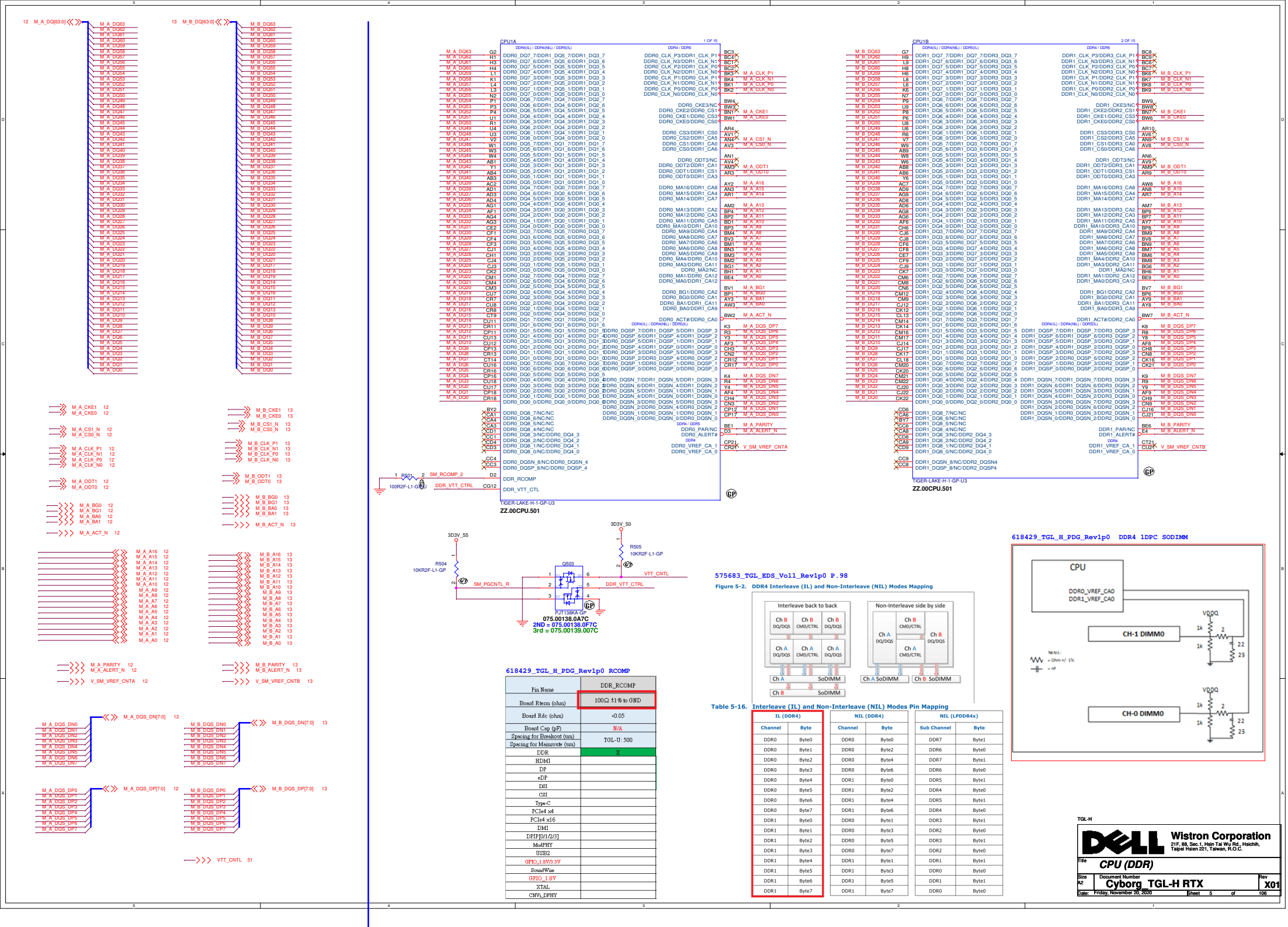

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Figure 5-2. DDR4 Interleave (IL) and Non-Interleave (NIL) Modes Mapping

618429_TGL_H_PDG_Rev1p0 RCOMP

Pin Name	DDR_RCOMP
Board Rterm (ohm)	100Ω ±1% to GND
Board Rdc (ohm)	<0.05
Board Cap (pF)	N/A
Spacing for Breakout (um)	TGL-U: 500
Spacing for Manuroute (um)	
DDR	X
HDMI	
DP	
eDP	
DSI	
CSI	
Type-C	
PCIe4 x4	
PCIe4 x16	
DMI	
DPIP[D/1/2/3]	
MoPHY	
USB2	
GPIO_1.8V/3.3V	
SoundWire	
GPIO_1.8V	
XTAL	
CNVi_DPHY	

Table 5-16. Interleave (IL) and Non-Interleave (NIL) Modes Pin Mapping

IL (DDR4)		NIL (DDR4)		NIL (LPDDR4x)	
Channel	Byte	Channel	Byte	Sub Channel	Byte
DDR0	Byte0	DDR0	Byte0	DDR7	Byte1
DDR0	Byte1	DDR0	Byte2	DDR6	Byte0
DDR0	Byte2	DDR0	Byte4	DDR7	Byte1
DDR0	Byte3	DDR0	Byte6	DDR6	Byte0
DDR0	Byte4	DDR1	Byte0	DDR5	Byte1
DDR0	Byte5	DDR1	Byte2	DDR4	Byte0
DDR0	Byte6	DDR1	Byte4	DDR5	Byte1
DDR0	Byte7	DDR1	Byte6	DDR4	Byte0
DDR1	Byte0	DDR0	Byte1	DDR3	Byte1
DDR1	Byte1	DDR0	Byte3	DDR2	Byte0
DDR1	Byte2	DDR0	Byte5	DDR3	Byte1
DDR1	Byte3	DDR0	Byte7	DDR2	Byte0
DDR1	Byte4	DDR1	Byte1	DDR1	Byte1
DDR1	Byte5	DDR1	Byte3	DDR0	Byte0
DDR1	Byte6	DDR1	Byte5	DDR1	Byte1
DDR1	Byte7	DDR1	Byte7	DDR0	Byte0

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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