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CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

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Engineer:	Surface	
Size: A3	Project Name: U22 DV1.3	Rev: 1.3.3
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Schematics Change History

Rev.	Date	Comments
0p9	28 Oct 2014	1. Starting with G_EV1_1021-1630.DSN 2. Added SL schematic from page 72 ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 3. Added External USB3 schematic from ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 4. Added external DP ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 5. Added IR_CAMERA from Front Camera...put in page 49 6. Removed page 73 PCIe GPU 7. Added Blade from T 8. Removed P72 T2B Pwr Transistors
0p10	3 Nov 2014	1. Changing to NVDC 2. Replaced GTX with GT, kept bypass caps 3. Replaced Charger with BQ24770
0p11	3 Nov 2014	1. Replace SKL-U with SKL-Y
0p12	11 Nov 2014	1. Model DDR connection from Intel SDS
0p13	18 Nov 2014	1. Added FUB information to all components 2. Changed Decretes.. sizing caps
0p14	20 Nov 2014	1. Added +5VA_SHA 2. Added T Cost Down/XCN's 3. Added SL +5V load Switch & Caps 4. Added Blade +5V load Switch & Caps
0p15	26 Nov 2014	1. Removed Boost 2. Re-adjusted usb ports on CPU 3. Removed Audio DSP
0p16	03 Dec 2014	1. changed +1VSB regulator 2. changed IR Camera/added diode 3. added power numbers from 0.91 PDG, Oct14 4. changed BLADE connector 5. cpu decoupling caps changed 6. changed +5V/+3V inductors (place holder)
0p17	05 Dec 2014	1. swapped M_A_CAA with MA_CAB on U1601/U1602 2. added two SAR chips, P32 3. remove tp's from csi lines on (p23) 4. change from 10 ceramic to 3 tantalum-poly on usb3 typeA (p45) 5. remove the RSENSE from output of +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) 6. change RSENSE input to 0402 from 0603 for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) input regulator 7. change inductor for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58) to HMLE20161B-1R0MDR-01 8. change RSENSE input to 0402 from 0603 for +5V_TS,+5V_SDXC,+5V_AUDIO,+5V, +5V_FAN(p64) 9. change RSENSE input to 0402 from 0603 for +3P3V_PANEL,+3P3V,+3P3V_SENSOR,+1P8V_DMIC (p65) 10. Replacing the SL connector with X908351-001 11. Replace PL5901 and PL5902 with CMLE042T-2R2MS-01 12. Replace 0402 1uf 6.3V with 0201 1uF 6.3V X5R 13. Replace L7201 with TOKO #A919CY-100M 14. Added VSYS -> BLADE FANG supply (p73)
0p18	09 Dec 2014	1. Reduced sizes of parts for Cameras (Resistors/Caps/Regulators)
0p19	12 Dec 2014	1. All 47uF caps become 0805/1mmZ 2. All 10uF caps become 0402...4V/6.3V
0p20	15 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x4 2. Shui Changes 3. more Shui Changes
0p21	16 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x5 2. changes from EV_schematic_issue_check_1216_JDM1.xlsx 3. changed name of +6_12 to +V_ALWAYS_ON 4. Removed 2 Mikes & Front Mike & added FPC conn 5. Added 2nd BLADE connector
0p22	17 Dec 2014	1. Replaced SD connector with AY531465T 2. changes from EV_schematic_issue_check_viola_1217_JDM1.xlsx
0p23 – current		1. See apexUfixes_revXpXX.xlsx

CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors

S = Short after design fixed

Property: BUILD-OPT

DNP = Not Installed Part.

Title:	CHANGE HISTORY-1		
Engineer:	*Surface*		
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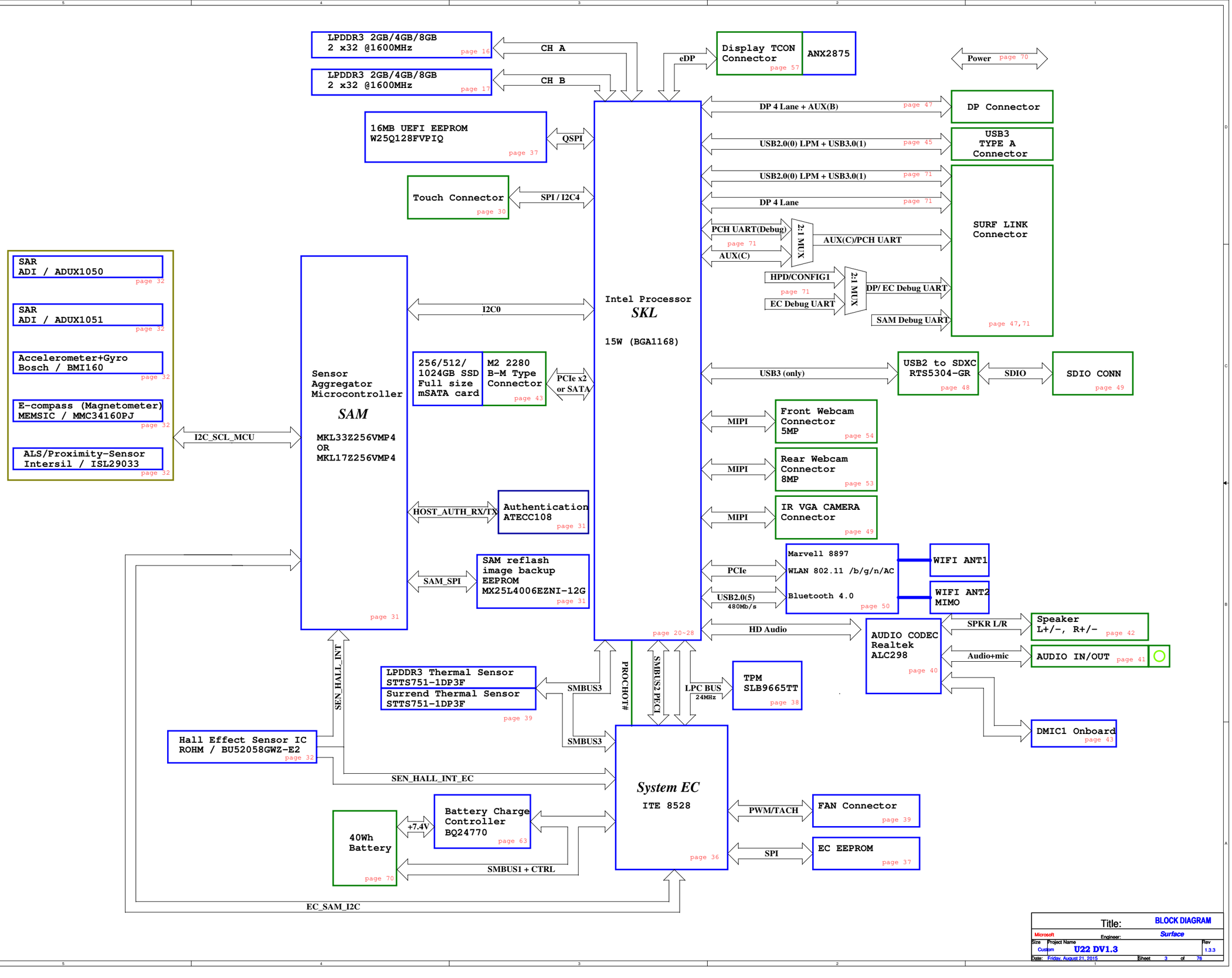
LPDDR3 2GB/4GB/8GB
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LPDDR3 2GB/4GB/8GB
2 x32 @1600MHz
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CH B
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SAR
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SMBUS3
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SMBUS1 + CTRL
EC_SAM_I2C
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Microsoft
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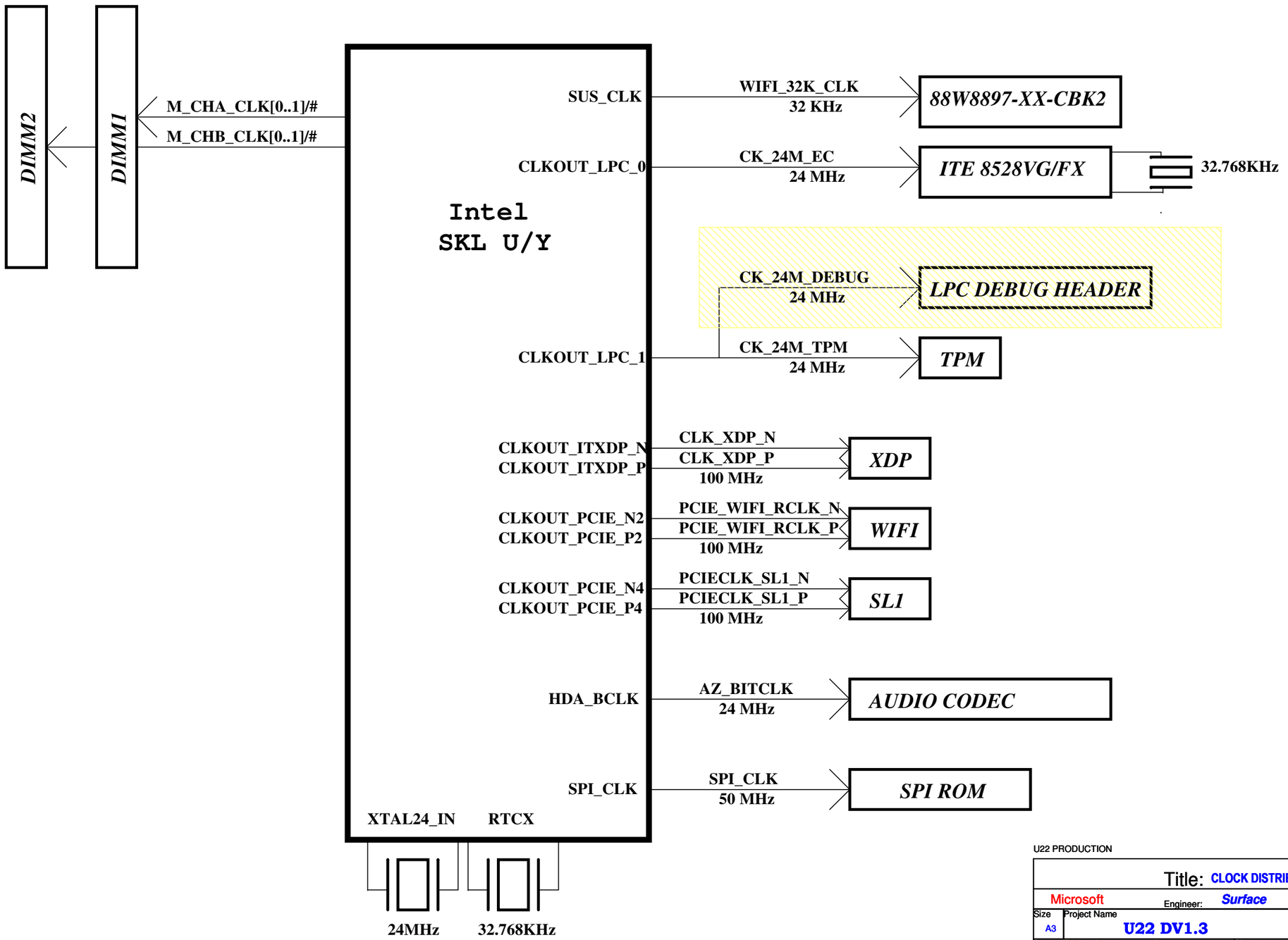
HSW Buffer Through Mode for Pre-Silicon



U22 PRODUCTION

Title: CLOCK DISTRIBUTION(TBD)		
Microsoft	Engineer: Surface	
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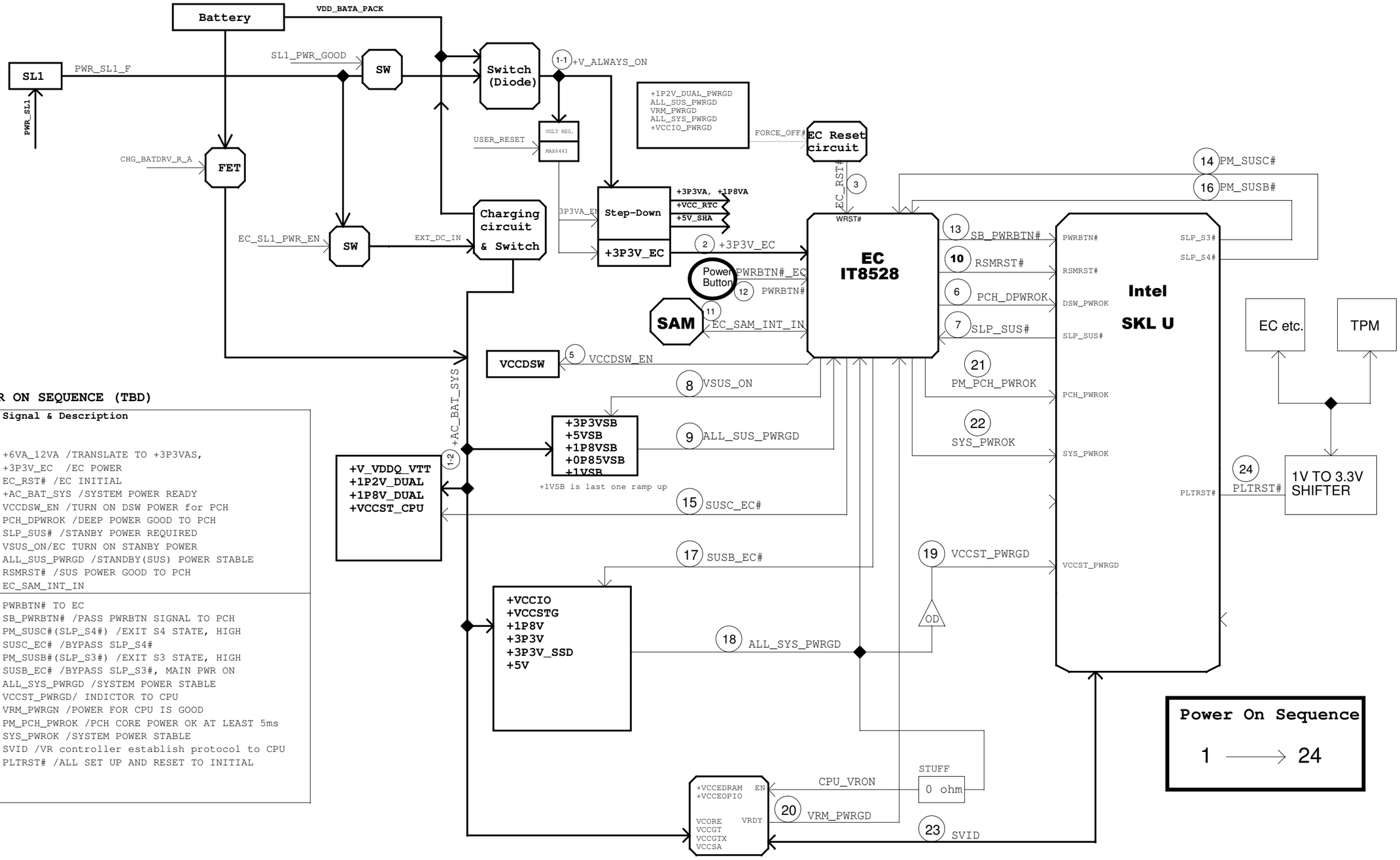

POWER ON SEQUENCE (TBD)

STEP	Signal & Description
1	+6VA_12VA /TRANSLATE TO +3P3VAS,
2	+3P3V_EC /EC POWER
3	EC_RST# /EC INITIAL
4.	+AC_BAT_SYS /SYSTEM POWER READY
5.	VCCDSW_EN /TURN ON DSW POWER for PCH
6.	PCH_DPWROK /DEEP POWER GOOD TO PCH
7.	SLP_SUS# /STANBY POWER REQUIRED
8.	VSUS_ON/EC TURN ON STANBY POWER
9.	ALL_SUS_PWRGD /STANDBY(SUS) POWER STABLE
10.	RSMRST# /SUS POWER GOOD TO PCH
11.	EC_SAM_INT_IN
12	PWRBTN# TO EC
13.	SB_PWRBTN# /PASS PWRBTN SIGNAL TO PCH
14.	PM_SUSC#(SLP_S4#) /EXIT S4 STATE, HIGH
15.	SUSC_EC# /BYPASS SLP_S4#
16.	PM_SUSB#(SLP_S3#) /EXIT S3 STATE, HIGH
17.	SUSB_EC# /BYPASS SLP_S3#, MAIN PWR ON
18.	ALL_SYS_PWRGD /SYSTEM POWER STABLE
19.	VCCST_PWRGD/ INDICTOR TO CPU
20.	VRM_PWRGN /POWER FOR CPU IS GOOD
21.	PM_PCH_PWROK /PCH CORE POWER OK AT LEAST 5ms
22.	SYS_PWROK /SYSTEM POWER STABLE
23.	SVID /VR controller establish protocol to CPU
24.	PLTRST# /ALL SET UP AND RESET TO INITIAL

U22 PRODUCTION

Microsoft	Title: SIGNAL&RESET MAP	Engineer: Surface	
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