Loveland Schematics
Skylake-U

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Variant Name>

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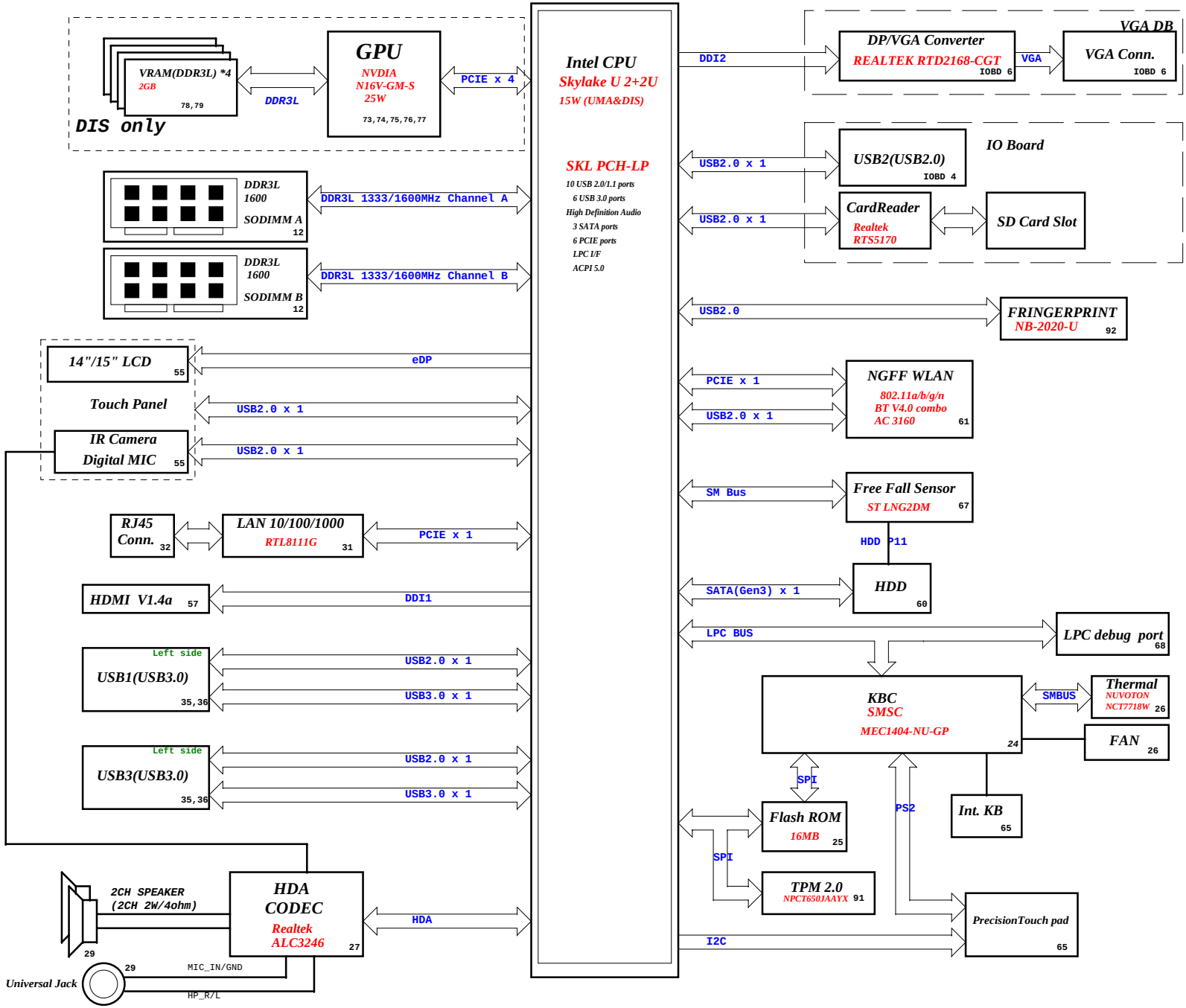
Project code:
Love14 SKL --> 4PD060010001
Love15 SKL --> 4PD061010001
PCB P/N: 14291
Revision: A00

Loveland SKL-U Block Diagram



CHARGER — BQ24780RUYR — 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC — RT6576DGQW — 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_PWR_2 5V_S5 3D3V_S5

CPU Core Power — NCP81208MNTXG / NCP81382MNTXG X2 / NCP81253MNTBG — 46~50

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCSA

DDR3L SUS — TPS51716RUKR — 51

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

CPU DCDC-V1D00A — SY8208DQNC — 53

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D5V — S-1339D15-M5001 — 54

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

LDO-V1D8V — APL5930KAI-TRG — 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 — G5016KD1U — 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

VCCSTG — M5938ARD1U — 40

INPUTS	OUTPUTS
5V_S5	+VCCIO +VCCSTG

VCCST — M5938ARD1U — 40

INPUTS	OUTPUTS
5V_S5	+V1.00U_CPU +VCCST_CPU

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Bottom

<Core Design>

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Main Func = CPU

(Blanking)

<Core Design>

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Title: *(Reserved)*

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Main Func = CPU

#544669 CRB Rev0.52

+VCCST_CPU

R419
1KR2J-1-GP

R420
DY
Do Not Stuff

PCH_THERMTRIP

H_THERMTRIP# [40]

+VCCSTG

+VCCSTG = 1.0 V

R401
1KR2J-1-GP
Rb

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

[24] H_PECI
[24,43,44,46] H_PROCHOT#

Do Not Stuff
R404
H_PROCHOT#_R_R
R403
499R2F-2-GP
Ra
Do Not Stuff

TP401
Do Not Stuff
TP402

H_CATERR#
H_PROCHOT#_R
PCH_THERMTRIP
SKTOCC#

[99] XDP_BPM[3:0]

XDP_BPM0
XDP_BPM1
XDP_BPM2
XDP_BPM3

#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm

Do Not Stuff
TP403
GPP_E3/CPU_GP0

[24,55] TOUCH_PANEL_INTR#
[24,65] INT_TP#

Do Not Stuff
R2045
TOUCHPAD_INTR#

Do Not Stuff
TP404
GPP_B4/CPU_GP3

CPU_POPIRCOMP
PCH_POPIRCOMP
49D9R2F-GP
R412
R413
49D9R2F-GP

CPU1D
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SKYLAKE_ULT

CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
CPU MISC
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

JTAG
PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#
PCH_JTAG_TCK
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_TRST#
JTAGX

XDP_TCLK [99]
XDP_TDI [99]
XDP_TDO_CPU [99]
XDP_TMS [99]
XDP_TRST# [99]
PCH_JTAG_TCK [99]
PCH_JTAG_TDI [99]
PCH_JTAG_TDO [99]
PCH_JTAG_TMS [99]
XDP_TRST# [99]
XDP_TCK_JTAGX [99]

SKYLAKE-GP-U
071.SKYLA.000U

+VCCSTG = 1.0 V

+VCCSTG

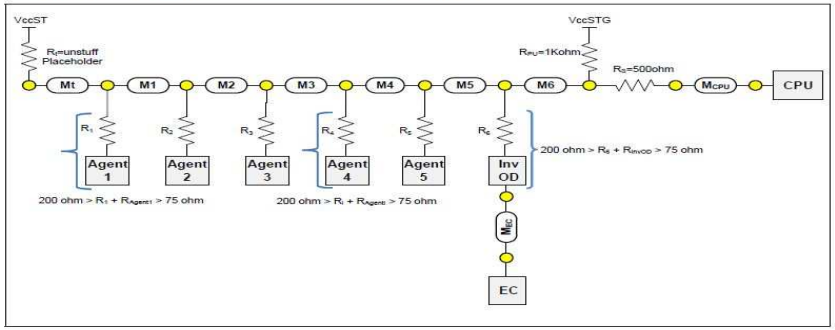
XDP_TMS
XDP_TDI
XDP_TDO_CPU
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
XDP_TCK_JTAGX

DY
Do Not Stuff
R421
R422
R423
51R2J-2-GP
R408
R409
R416
R417

XDP_TRST#
XDP_TCLK
PCH_JTAG_TCK
R402
R406
R407
DY
Do Not Stuff
51R2J-2-GP
Do Not Stuff

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

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Title	CPU_(JTAG/CPU SIDE BAND)	
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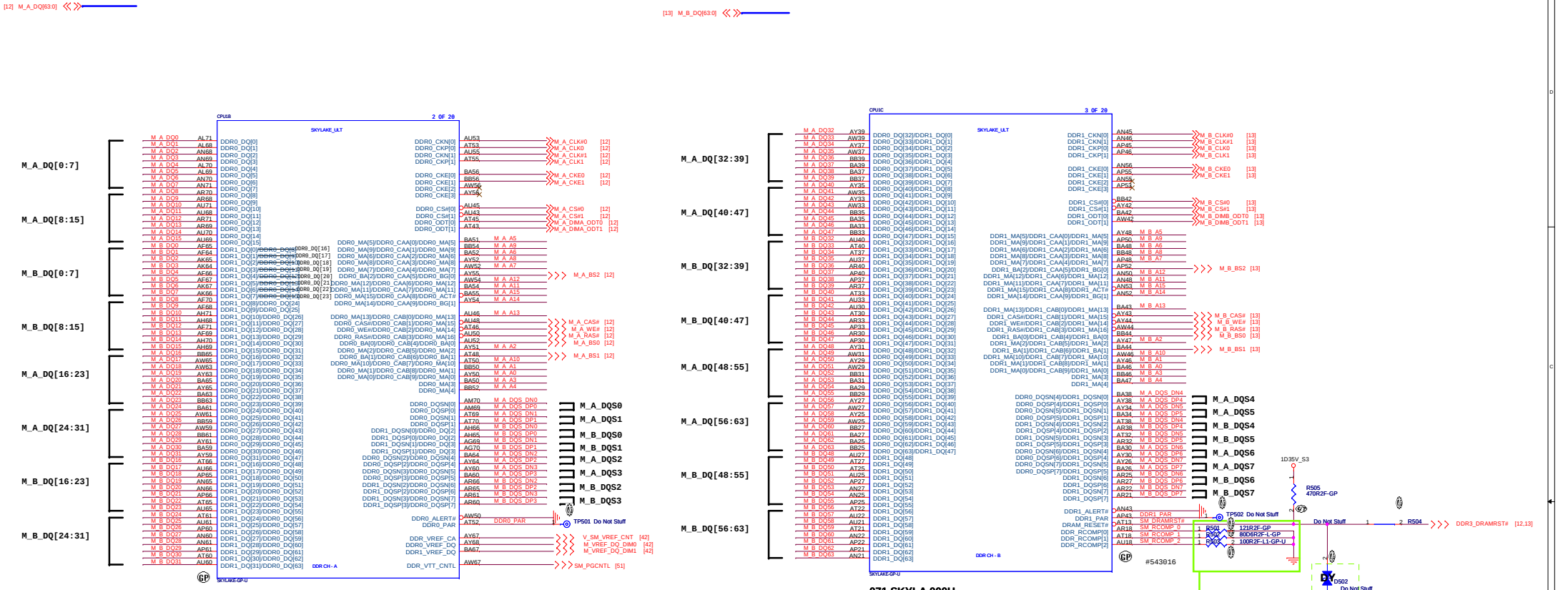
Main Func = CPU

DDR3L ball type: Interleaved Type



071.SKYLA.000U

071.SKYLA.000U

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0] DDR1_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT . Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
	DDR3L SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - SKL-Y LPDDR3, RVP5 - SKL-U LPDDR3)
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RTT NOM is defined by BIOS as High-Z in both ranks, when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z)
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.

<Core Design>

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Title: CPU (DDR)

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