



# Compal Confidential

## VIWZ1/VIWZ2 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

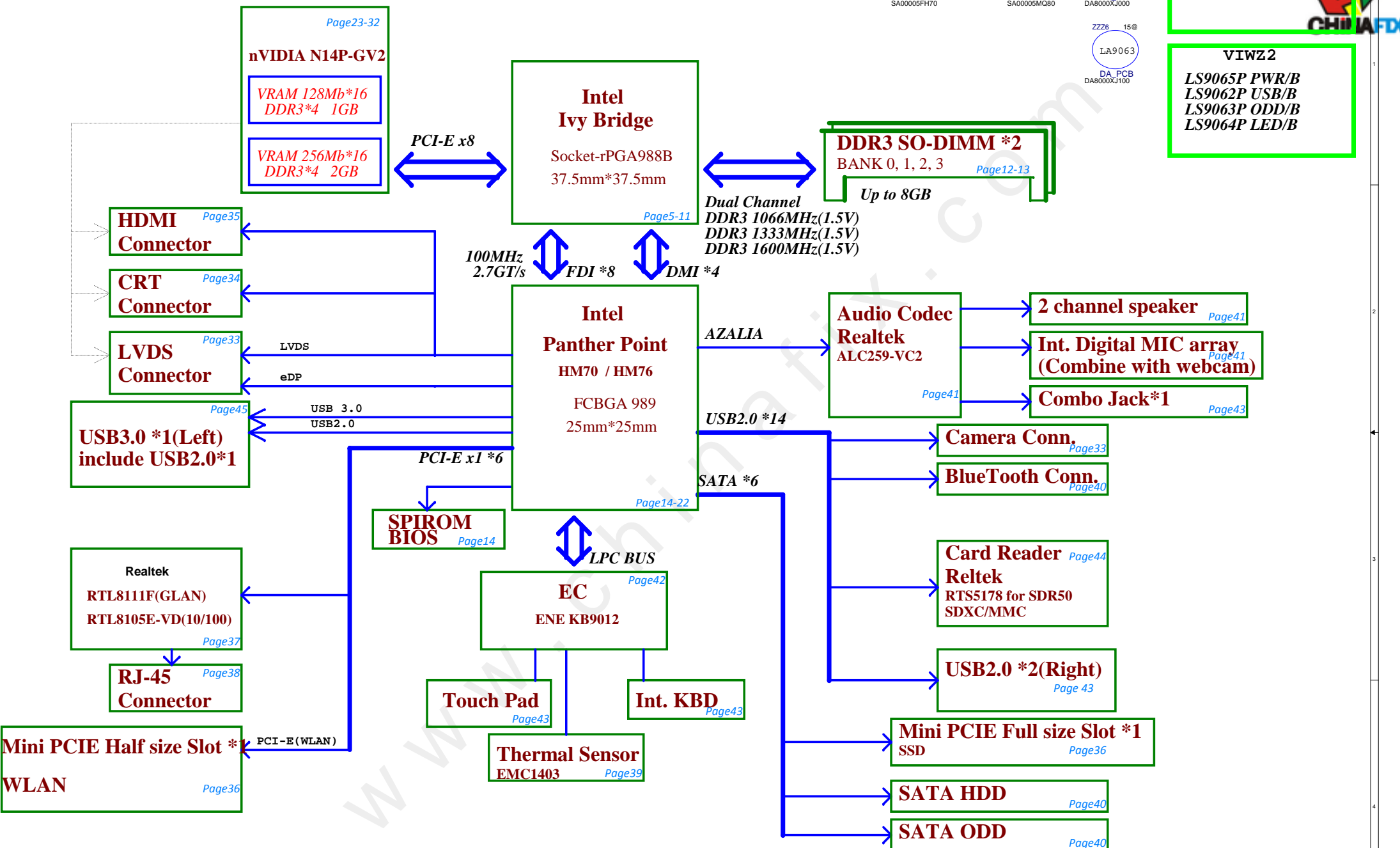
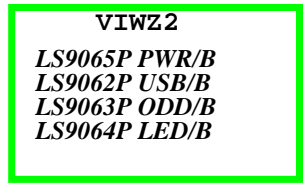
nVIDIA N14P-GV2

2012-12-26

LA-9063P

REV:1.0

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### Voltage Rails

power plane	+B	+5VALW	+1.5V	+3VALW	+5VS
					+3VS
State	○	○	○	○	+1.5VS
					+V1.05S_VCCP
S0	○	○	○	○	+VCC_CORE
					+VGA_CORE
S3	○	○	○	○	+VCC_GFXCORE_AXG
					+1.8VS
S5 S4/AC	○	○	○	○	+0.75VS
					+1.05VS
S5 S4/ Battery only	○	○	○	○	
S5 S4/AC & Battery don't exist	○	○	○	○	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### BOARD ID Table

Board ID	PCB Revision
0	LA-9061P 1.0
1	LA-9061P 0.3
2	LA-9061P 0.2
3	LA-9061P 0.1
4	LA-9063P 0.2
5	LA-9063P 0.2 TS
6	
7	

### Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%					
Ra/Rc/Re	100K +/- 5%					
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Project	Phase
0	0	0 V	0 V	0 V	2-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	2-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	2-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	2-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Re-flash	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Reserved	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Reserved	PVT
7	NC	2.500 V	3.300 V	3.300 V	Reserved	MP

### EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403	1001_101xb
USB Charger	1010 111X b		

### PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

### NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

### USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	Touch Screen
		2	Blue Tooth
EHCI1	UHCI1	3	Camera
		4	
		5	
EHCI1	UHCI2	6	
		7	
		8	USB Port (Right Side USB-BD)
EHCI2	UHCI3	9	USB Port (Right Side USB-BD)
		10	Mini Card(WLAN)
		11	Card Reader
EHCI2	UHCI4	12	
		13	

### BOM Structure Table

BTO Item	BOM Structure
GPU:N14P-GV2	GV2@
OPTIMUS part	OPT@
integrate Graphic part	UMA@
GPU:N14P-GV2 Strap	GV2@
GPU:N14P-GV2 GC6 function	GC6@
OPTIMUS no support GCLK	OPTNOGCLK@
OPTIMUS support GCLK	OPTGCLK@
Support Green CLK	GCLK@
not Support Green CLK	NOGCLK@
Support Green CLK 244	GCLK244@
Support Green CLK 304	GCLK304@
Cardreader	CR@
Support HP Woofer	woofer@
Gastube	Gastube@
EC RESET function	RESET@
HDMI	HDMI@
BlueTooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8105@
GIGA LAN	GIGA@
Deep Sleep S3	DS3@
Not Support Deep Sleep S3	NODS3@
ISCT	AOAC@
ISCT not support	NOAOAC@
Camera	CMOS@
For Z490 (14")	14@
For Z590 (15")	15@
Unpop	@
USB Charger	CHG@
not USBCharger	NOCHG@
Keyboard Back Light	KBL@
Touch Screen	TS@
HM76 by PCH	HM76@
HM70 by PCH	HM70@
Cardreader RTS5178	RTS5178@
Cardreader RTS5170	RTS5170@
for 14" Touch Screen	TS_14@
for 15" Touch Screen	TS_15@

### GPU BOM Structure Table

BOM Structure	N14P-GV2
OPT@	V
OPTNOGCLK@	V
GV2@	V
GC6@	Select

### SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	TP
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X	X
SMB_EC_DA1	+3VALW	X	+3VALW	X	X	X	X	X	X
SMB_EC_CK2	KB9012	X	X	X	X	X	X	X	X
SMB_EC_DA2	+3VALW	X	X	X	X	X	X	X	X
SMBCLK	PCH	X	X	X	V	V	X	X	V
SMBDATA	+3VALW	X	X	X	+3VS	+3VS	X	X	+3VS
SML0CLK	PCH	X	X	X	X	X	X	X	X
SML0DATA	+3VALW	X	X	X	X	X	X	X	X
SML1CLK	PCH	X	X	X	X	X	X	X	X
SML1DATA	+3VALW	+3VS	X	+3VS	X	X	+3VS	X	X

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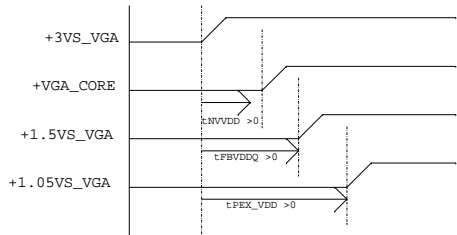
### VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	I	H	GC6_FB_CLAMP
GPIO1	OUT	-	MEM_VDD_CTL
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	RESERVED
GPIO6	OUT	L	GC6_FB_REQ
GPIO7	OUT	-	3DVision
GPIO8	I/O	L	Thermal Catastrophic Over Temperature
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	PWM_VID
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	PSI
GPIO14	OUT	N/A	
GPIO15	IN		
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		
GPIO19	IN	N/A	

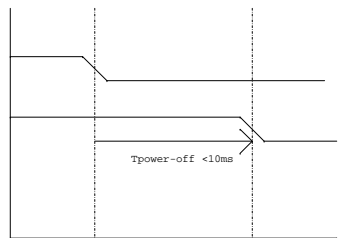
### Performance Mode P0 TDP at Tj = 102 C\* (GDDR3)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V



- all power rail ramp up time should be larger than 40us
- Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



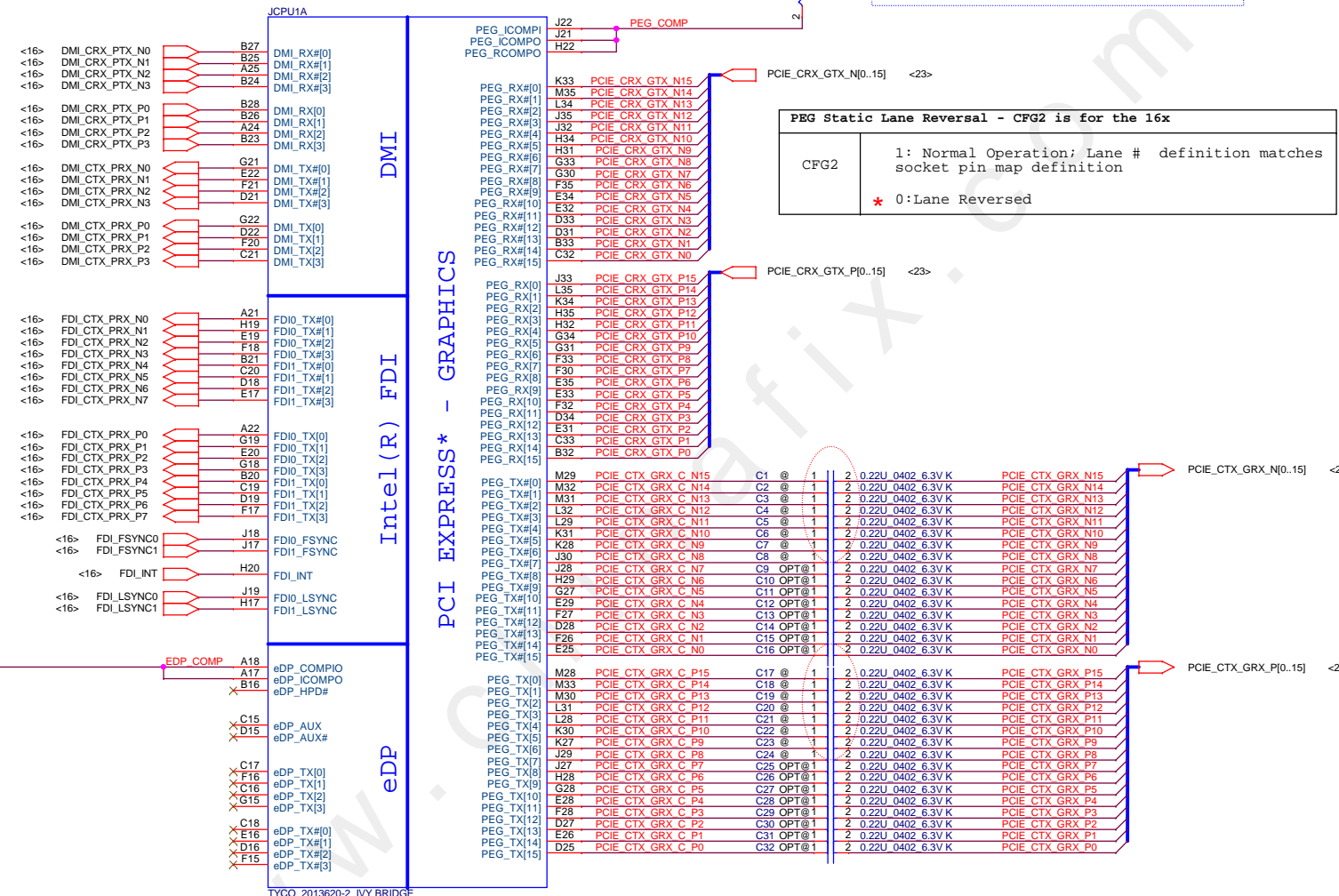
- all GPU power rails should be turned off within 10ms

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PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

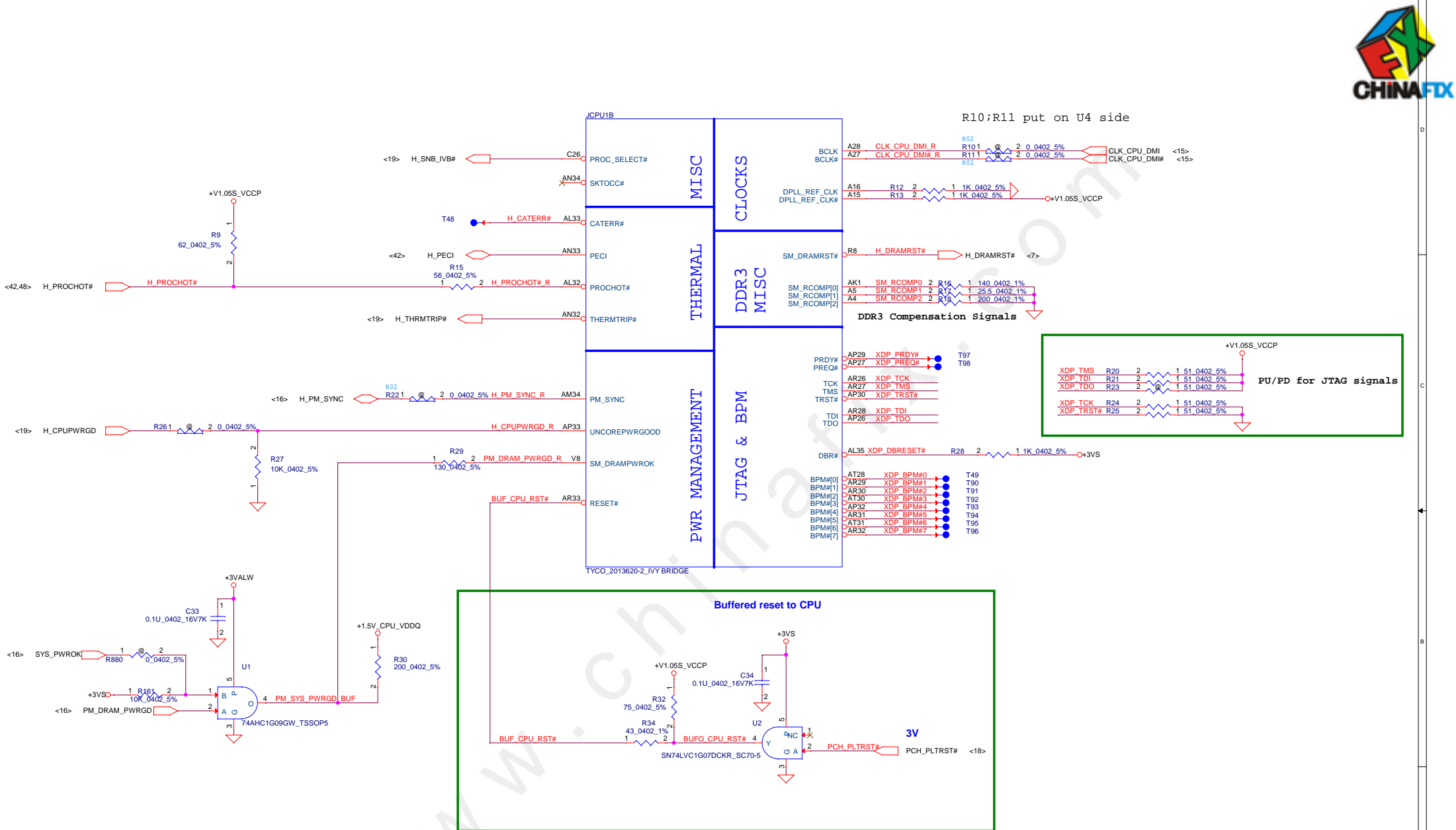


**PEG Static Lane Reversal - CFG2 is for the 16x**

CFG2	Definition
1	Normal Operation; Lane # definition matches socket pin map definition
* 0	Lane Reversed

eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

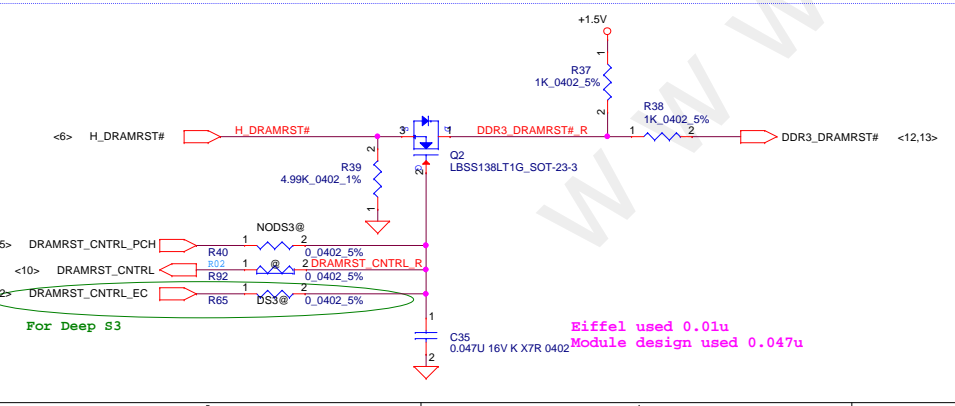
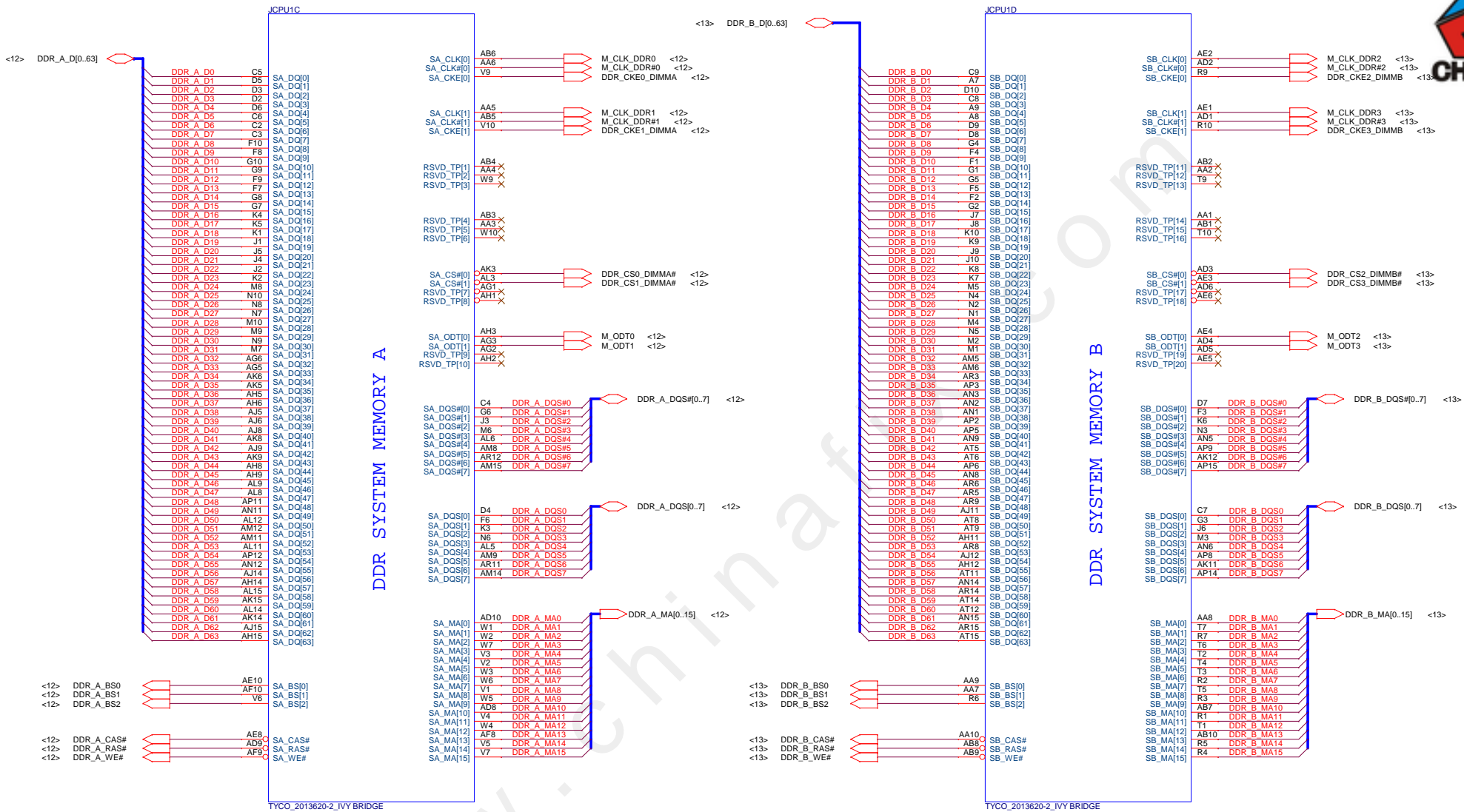
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Issued Date	2012/12/26	Deciphered Date	2012/07/11	PROCESSOR(1/7) DMI,FDI,PEG	
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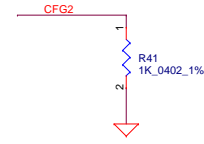
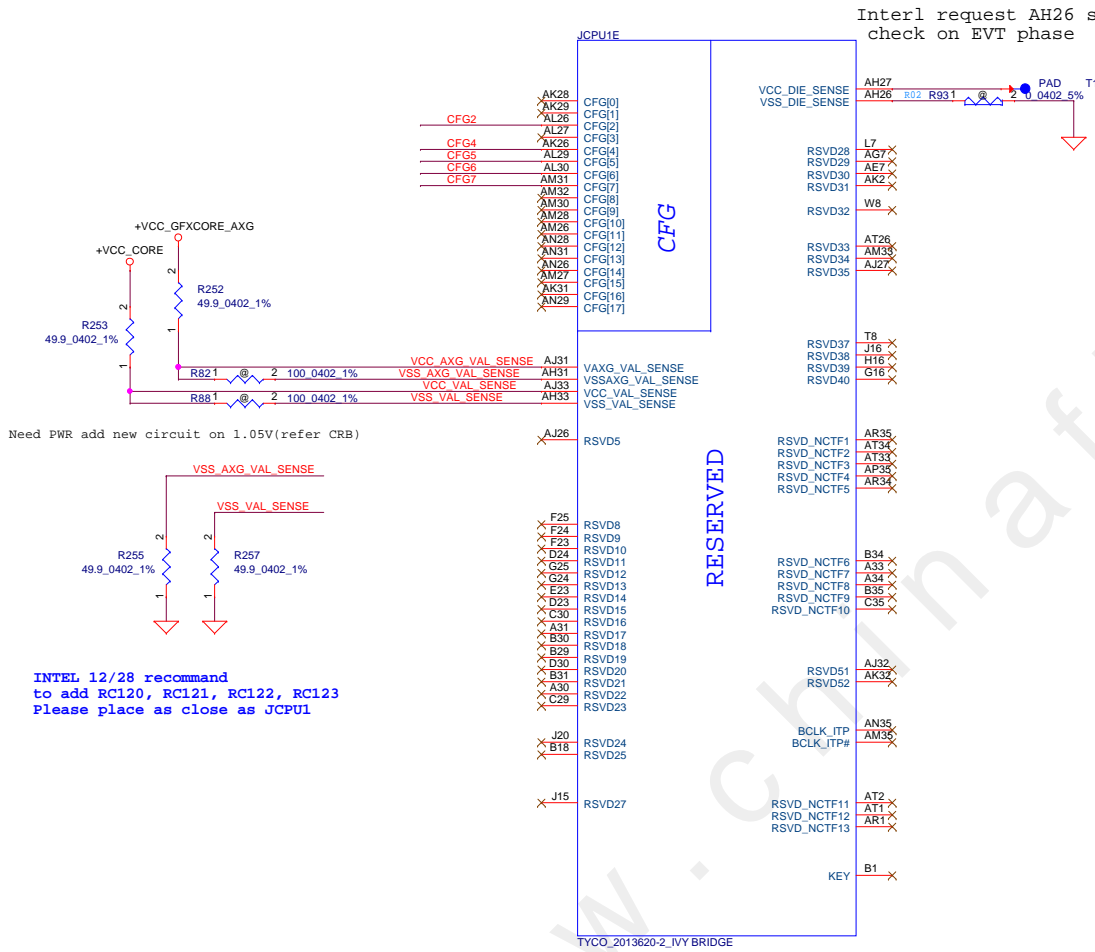
Title		Compal Electronics, Inc.	
PROCESSOR(2/7) PM,XDP,CLK			
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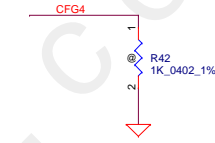
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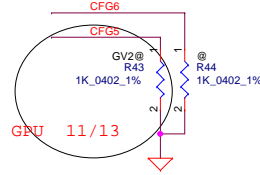
# CFG Straps for Processor



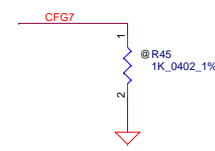
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRSETB de assertion 0: PEG Wait for BIOS for training





**POWER**

+VCC\_CORE  
 QC=94A  
 DC=53A

+V1.05S\_VCCP  
 8.5A

JCPU1F

**CORE SUPPLY**

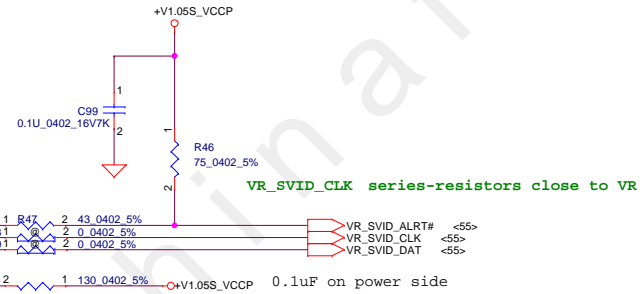
**PEG AND DDR**

**SVID**

**SENSE LINES**

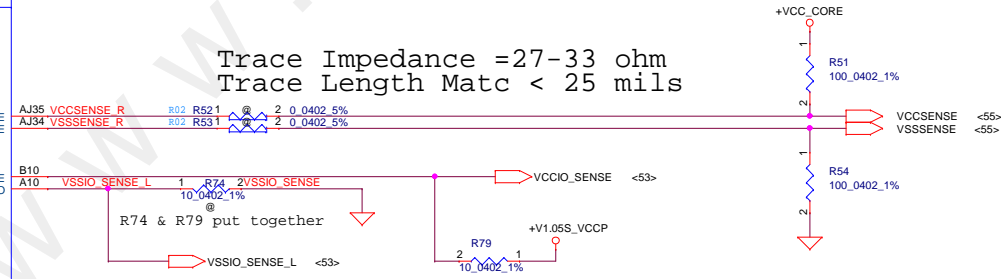
- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- VCC4
- AG31 VCC5
- AG29 VCC6
- AG28 VCC7
- AG27 VCC8
- AG26 VCC9
- AF35 VCC10
- AF34 VCC11
- AF33 VCC12
- AF32 VCC13
- AF31 VCC14
- AF30 VCC15
- AF29 VCC16
- AF28 VCC17
- AF27 VCC18
- AF26 VCC19
- AD35 VCC20
- AD34 VCC21
- AD33 VCC22
- AD32 VCC23
- AD31 VCC24
- AD30 VCC25
- AD29 VCC26
- AD28 VCC27
- AD27 VCC28
- AD26 VCC29
- AC35 VCC30
- AC34 VCC31
- AC33 VCC32
- AC32 VCC33
- AC31 VCC34
- AC30 VCC35
- AC29 VCC36
- AC28 VCC37
- AC27 VCC38
- AC26 VCC39
- AA35 VCC40
- AA34 VCC41
- AA33 VCC42
- AA32 VCC43
- AA31 VCC44
- AA30 VCC45
- AA29 VCC46
- AA28 VCC47
- AA27 VCC48
- AA26 VCC49
- Y35 VCC50
- Y34 VCC51
- Y33 VCC52
- Y32 VCC53
- Y31 VCC54
- Y30 VCC55
- Y29 VCC56
- Y28 VCC57
- Y27 VCC58
- Y26 VCC59
- V35 VCC60
- V34 VCC61
- V33 VCC62
- V32 VCC63
- V31 VCC64
- V30 VCC65
- V29 VCC66
- V28 VCC67
- V27 VCC68
- V26 VCC69
- U35 VCC70
- U34 VCC71
- U33 VCC72
- U32 VCC73
- U31 VCC74
- U30 VCC75
- U29 VCC76
- U28 VCC77
- U27 VCC78
- U26 VCC79
- R35 VCC80
- R34 VCC81
- R33 VCC82
- R32 VCC83
- R31 VCC84
- R30 VCC85
- R29 VCC86
- R28 VCC87
- R27 VCC88
- R26 VCC89
- P35 VCC90
- P34 VCC91
- P33 VCC92
- P32 VCC93
- P31 VCC94
- P30 VCC95
- P29 VCC96
- P28 VCC97
- P27 VCC98
- P26 VCC99
- VCC100

- VCCI01 AH13
- VCCI02 AH10
- VCCI03 AG10
- VCCI04 AC10
- VCCI05 Y10
- VCCI06 U10
- VCCI07 P10
- VCCI08 L10
- VCCI09 J14
- VCCI10 J13
- VCCI11 J12
- VCCI12 VCCI11
- VCCI13 J11
- VCCI14 H14
- VCCI15 H12
- VCCI16 H11
- VCCI17 G14
- VCCI18 G13
- VCCI19 G12
- VCCI20 F14
- VCCI21 F13
- VCCI22 F12
- VCCI23 F11
- VCCI24 E14
- VCCI25 E12
- VCCI26 E11
- VCCI27 D14
- VCCI28 D13
- VCCI29 D12
- VCCI30 D11
- VCCI31 C14
- VCCI32 C13
- VCCI33 C12
- VCCI34 C11
- VCCI35 B14
- VCCI36 B12
- VCCI37 A14
- VCCI38 A13
- VCCI39 A11
- VCCI40 J23



VCC\_SENCE 100ohm +-1% pull-up to VCC near processor

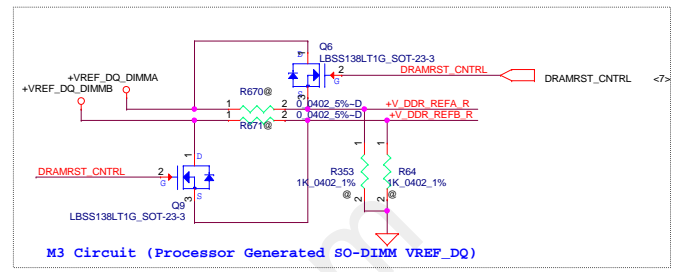
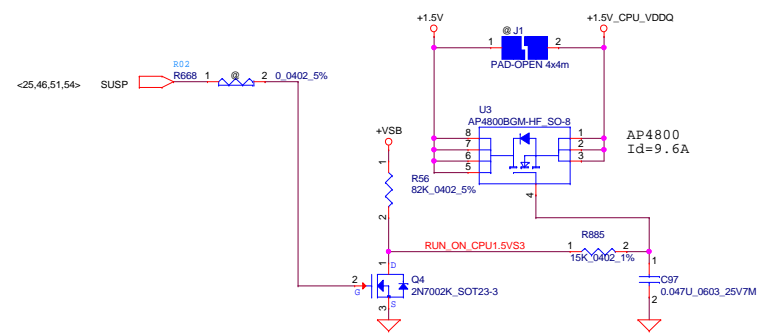
Trace Impedance =27-33 ohm  
 Trace Length Matc < 25 mils



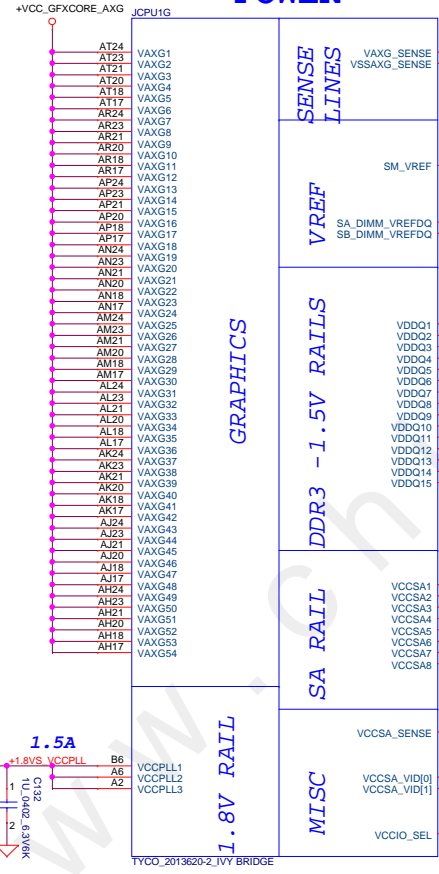
VSS\_SENCE 100ohm +-1% pull-down to GND near processor

TYCO\_2013620-2\_IVY BRIDGE

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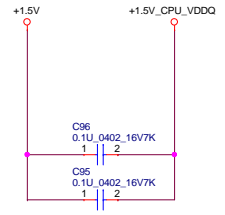
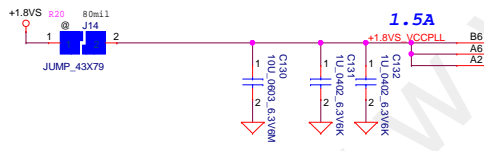


**POWER**

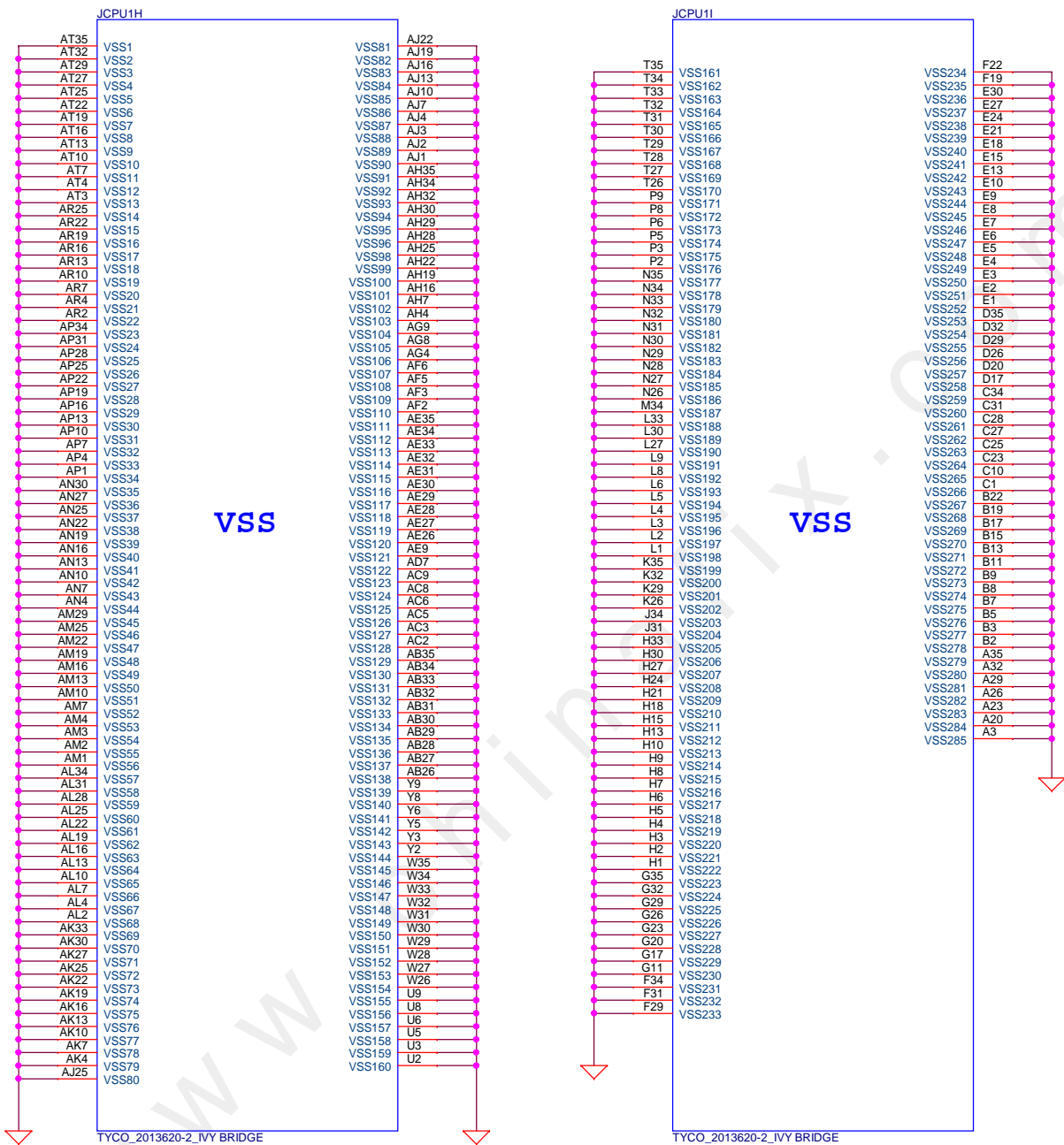


+V\_SM\_VREF should have 20 mil trace width

Q5-original part  
AP2302GN-HF\_SOT23-3  
SB523020210



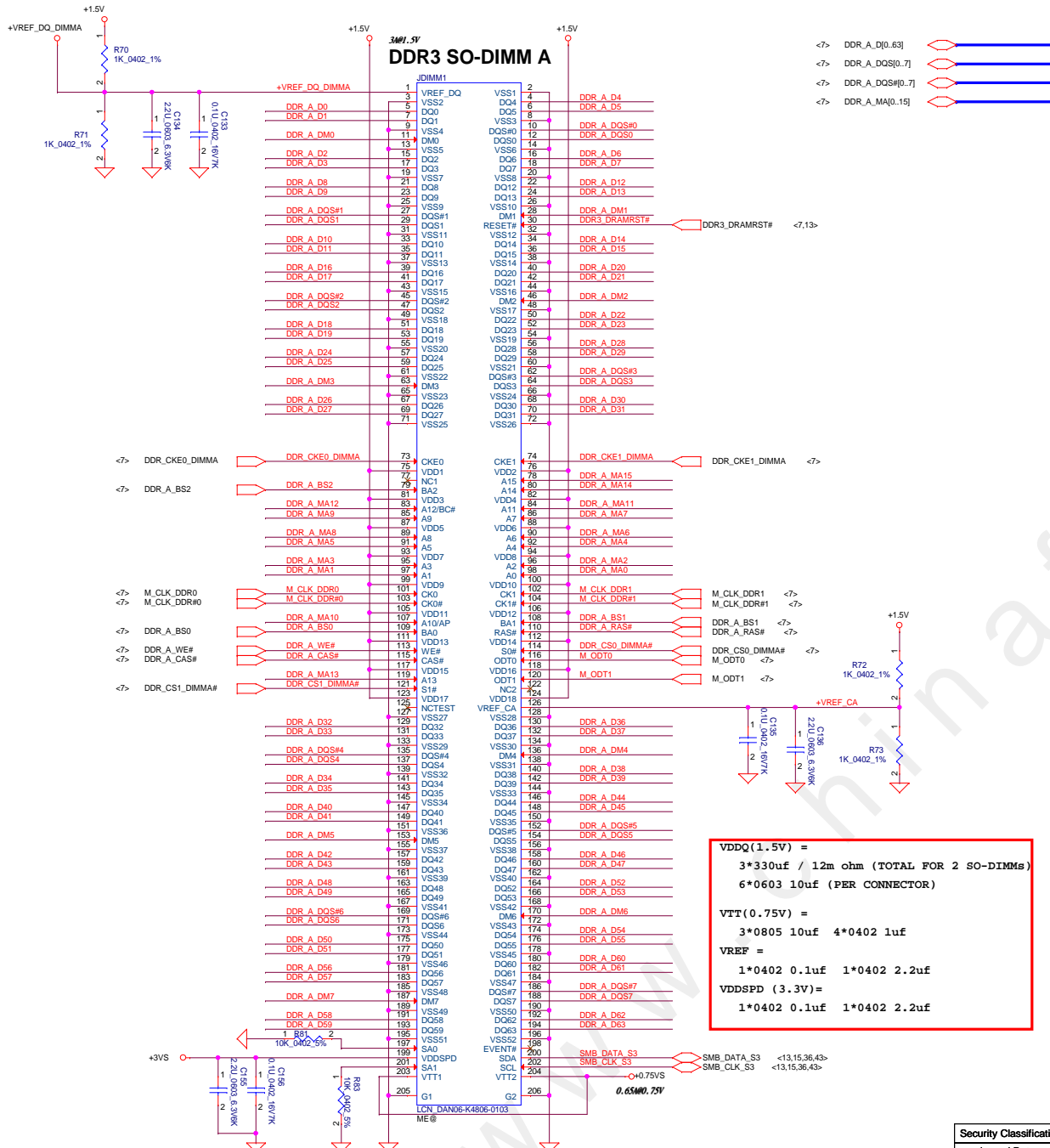
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VSS

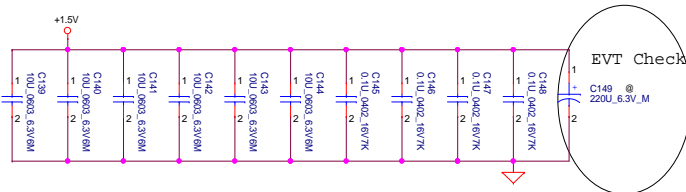
VSS

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OSCAN (220uF\_6.3V\_4.2L\_ESR17m)\*1=(SF00002Y00)  
 (10uF\_0603\_6.3V)\*8  
 (0.1uF\_402\_10V)\*4

Layout Note:  
Place near DIMM



VDDQ(1.5V) =  
 3\*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMS)  
 6\*0603 10uf (PER CONNECTOR)

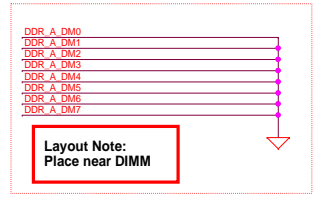
VTT(0.75V) =  
 3\*0805 10uf 4\*0402 1uf

VREF =  
 1\*0402 0.1uf 1\*0402 2.2uf

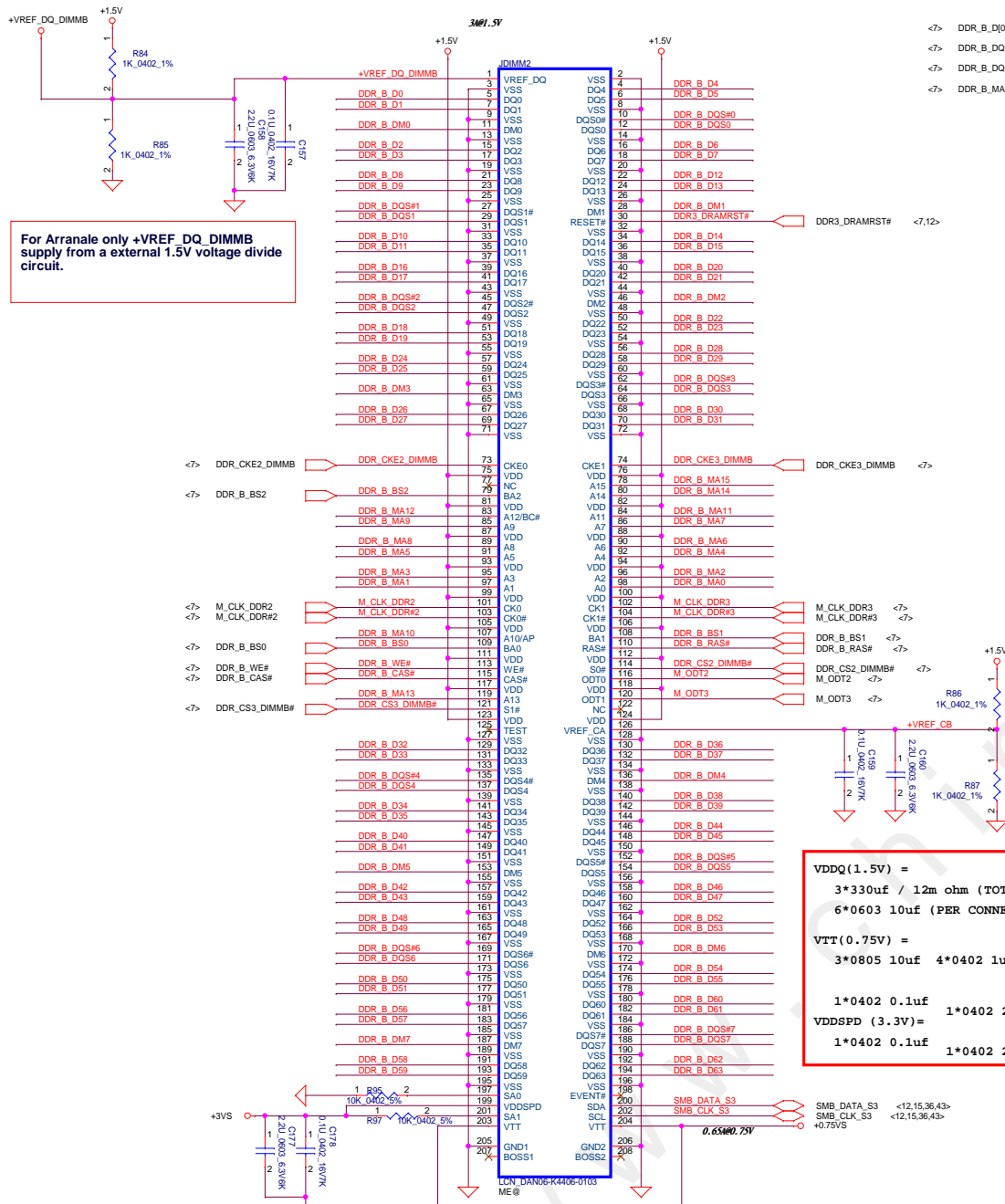
VDDSPD (3.3V) =  
 1\*0402 0.1uf 1\*0402 2.2uf

Layout Note:  
Place near DIMM

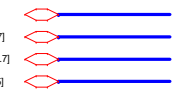
7/28 Update connect GND directly



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Revision 1.0 Sheet 12 of 62				



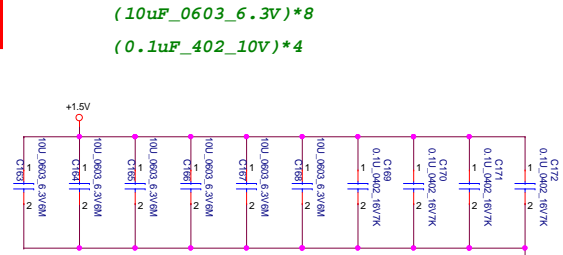
For Arranale only +VREF\_DQ\_DIMMB supply from an external 1.5V voltage divide circuit.



Layout Note: Place near DIMM

$$(10\mu F_{0603\_6.3V}) * 8$$

$$(0.1\mu F_{402\_10V}) * 4$$

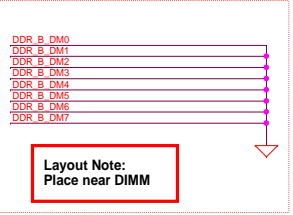
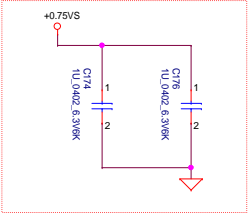


VDDQ(1.5V) =  
 $3 * 330\mu f / 12m\ ohm$  (TOTAL FOR 2 SO-DIMMs)  
 $6 * 0603\ 10\mu f$  (PER CONNECTOR)

VTT(0.75V) =  
 $3 * 0805\ 10\mu f$     $4 * 0402\ 1\mu f$

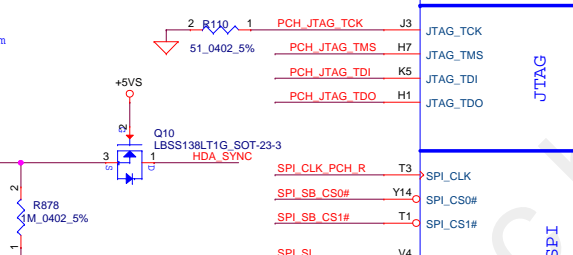
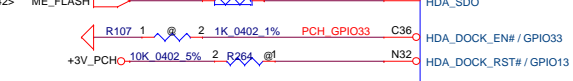
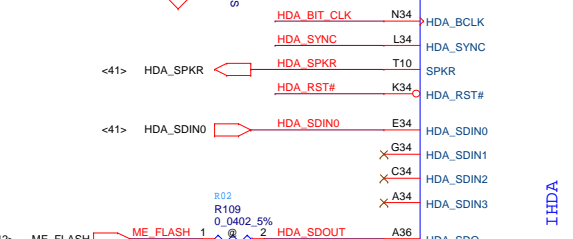
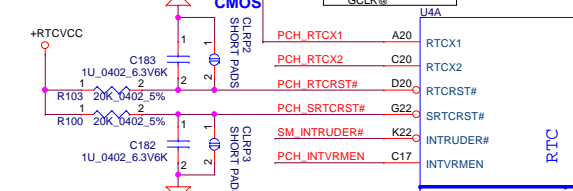
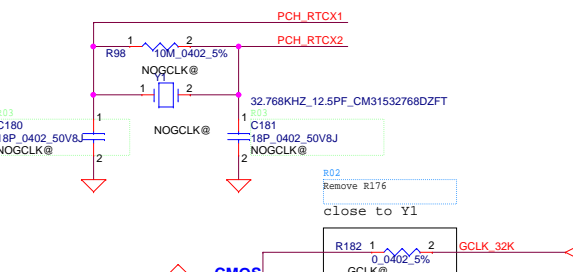
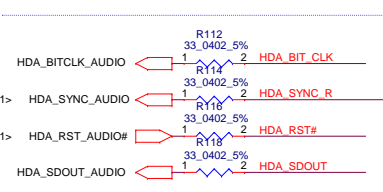
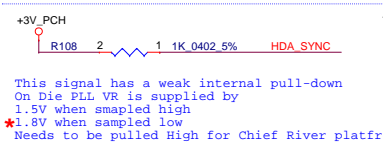
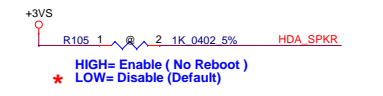
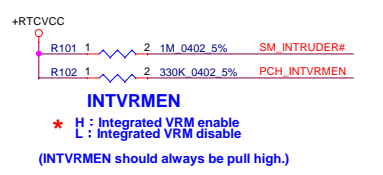
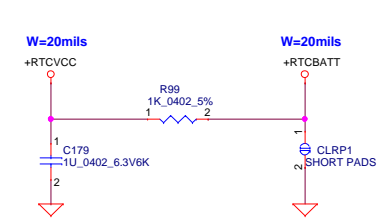
VDDSPD (3.3V) =  
 $1 * 0402\ 0.1\mu f$     $1 * 0402\ 2.2\mu f$   
 $1 * 0402\ 0.1\mu f$     $1 * 0402\ 2.2\mu f$

Layout Note: Place near DIMM

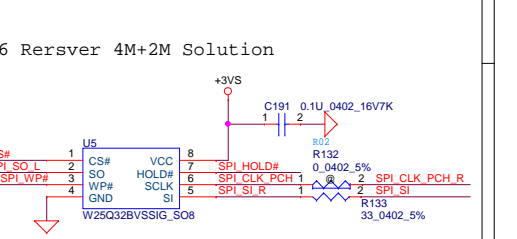
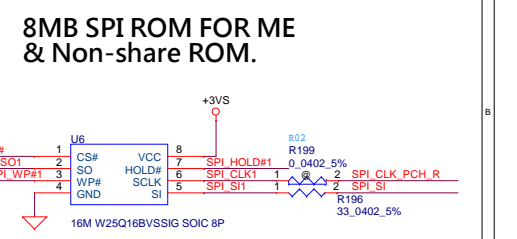
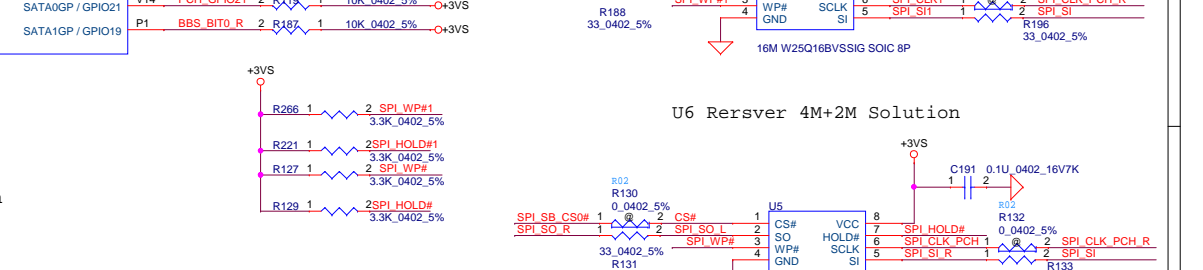
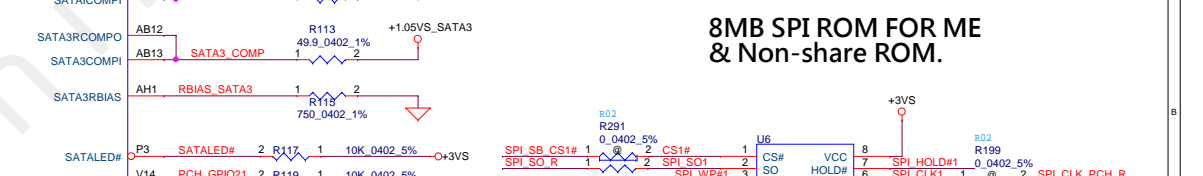
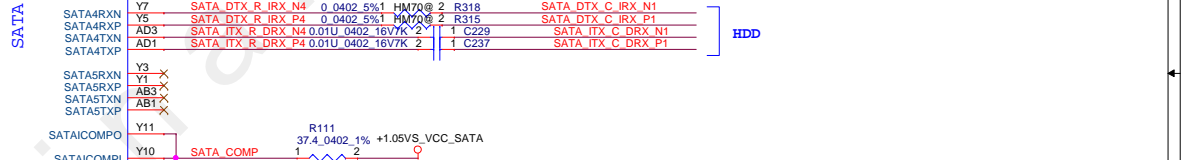
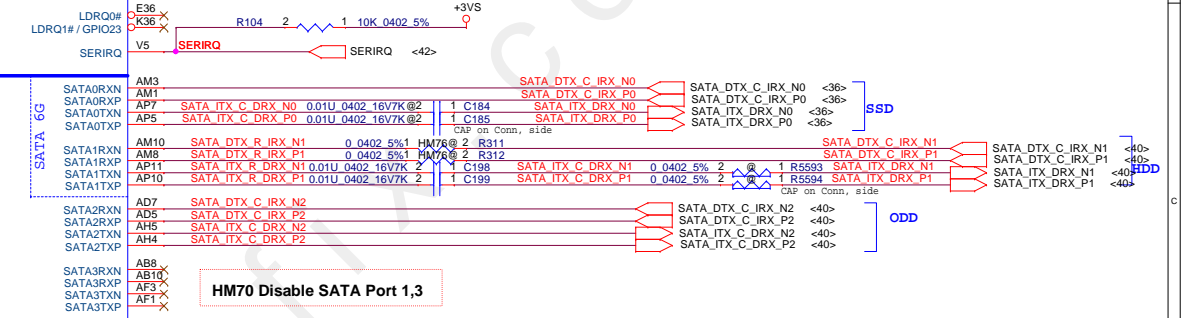
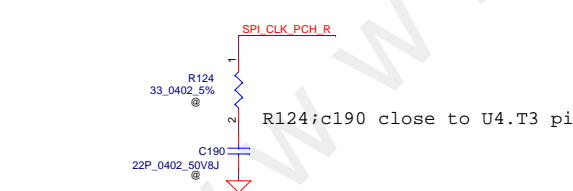


Layout Note: Place near DIMM

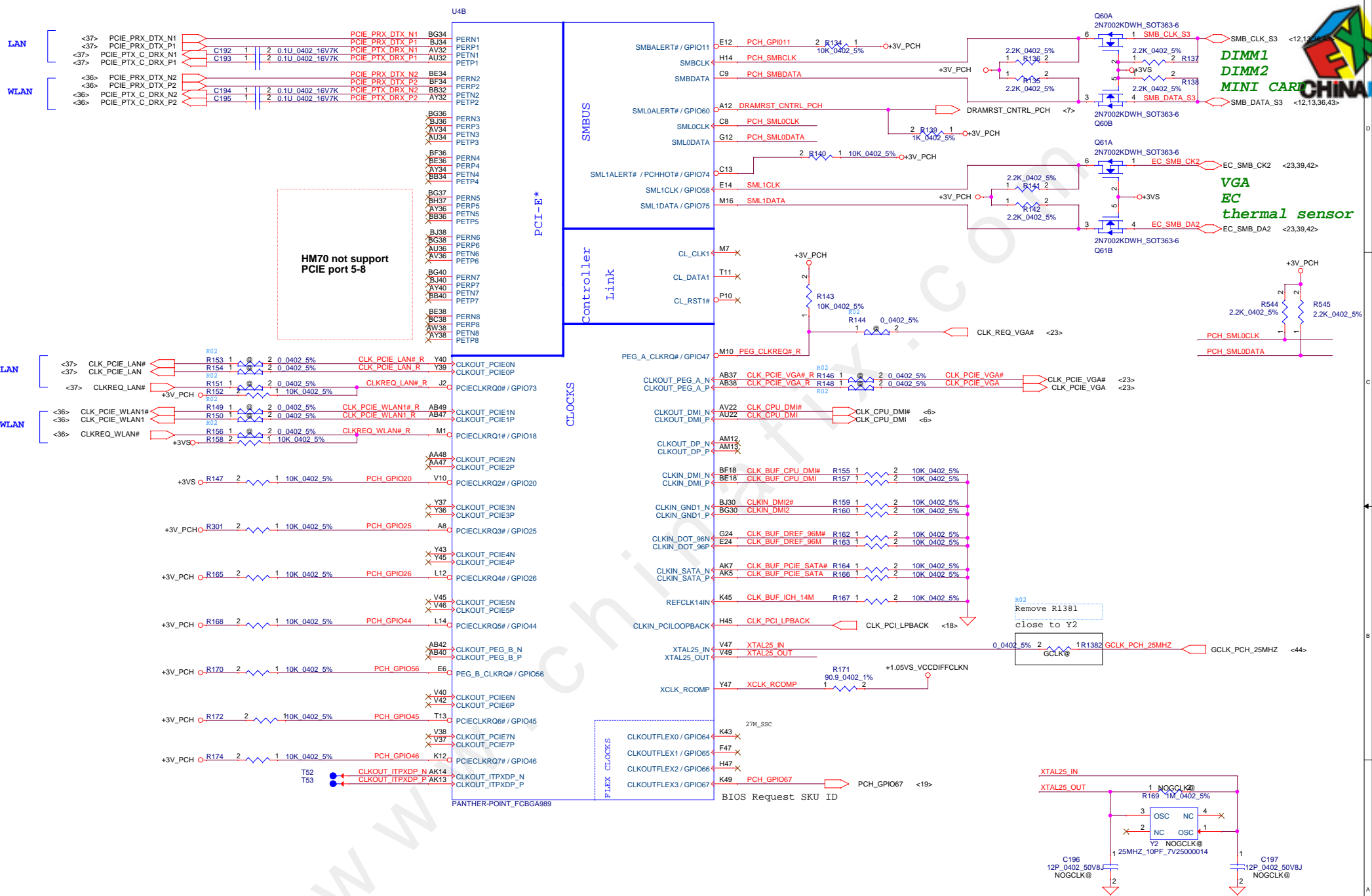
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Size	Document Number	Rev	LA-9603P	
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check with vender  
 Del Q10 check with codec  
 VDDIO using 3VALW

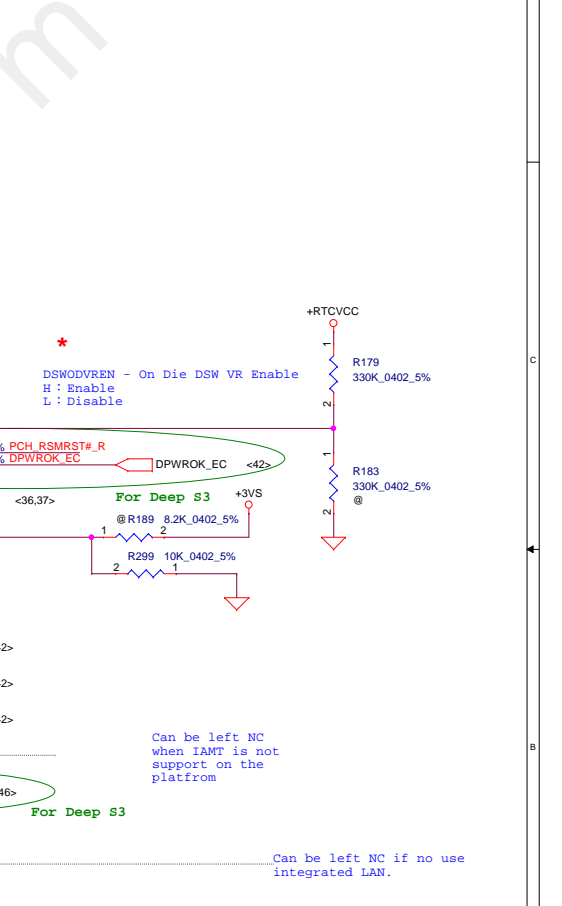
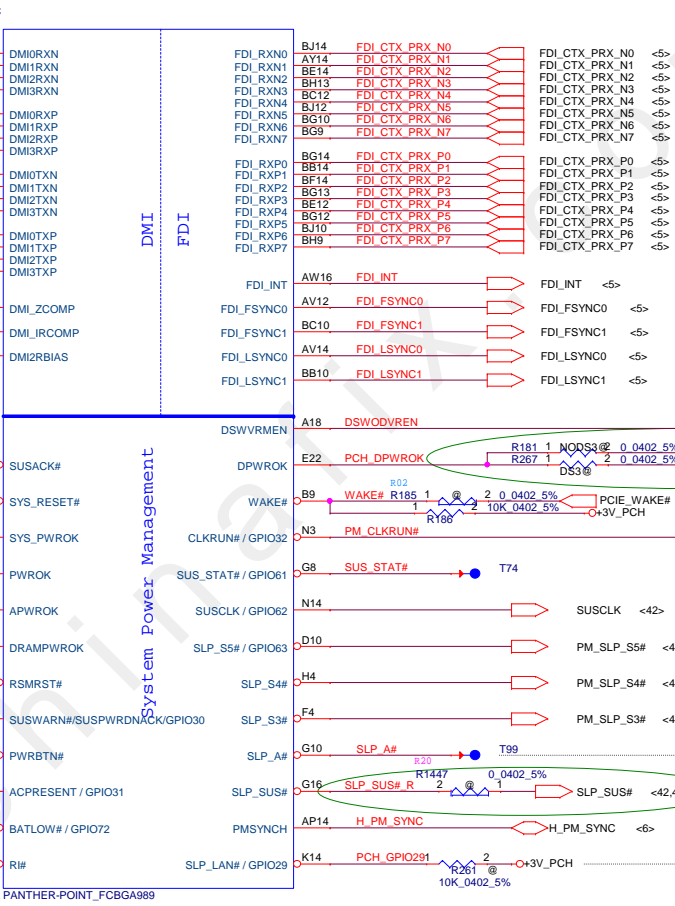
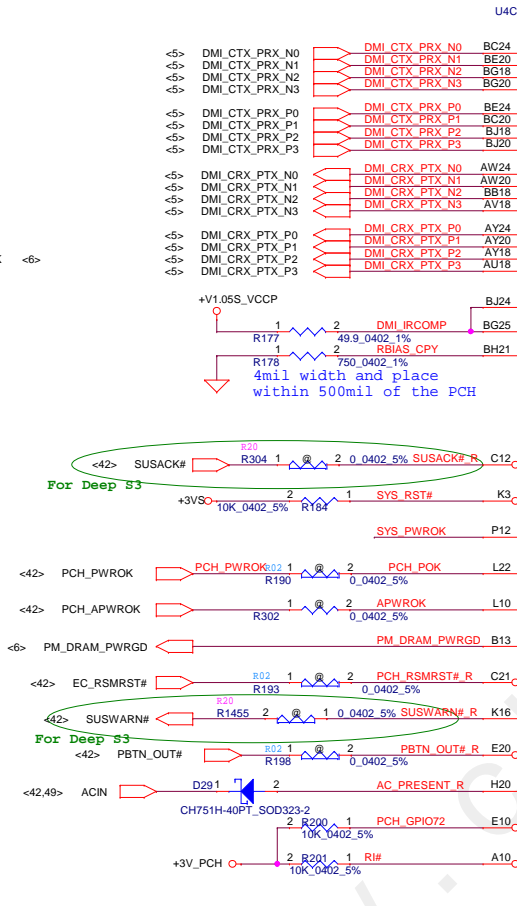
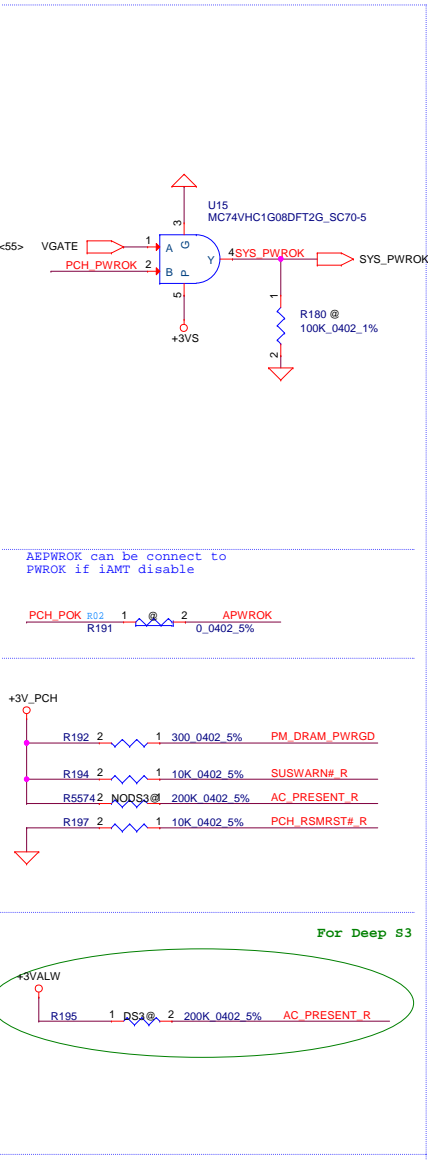


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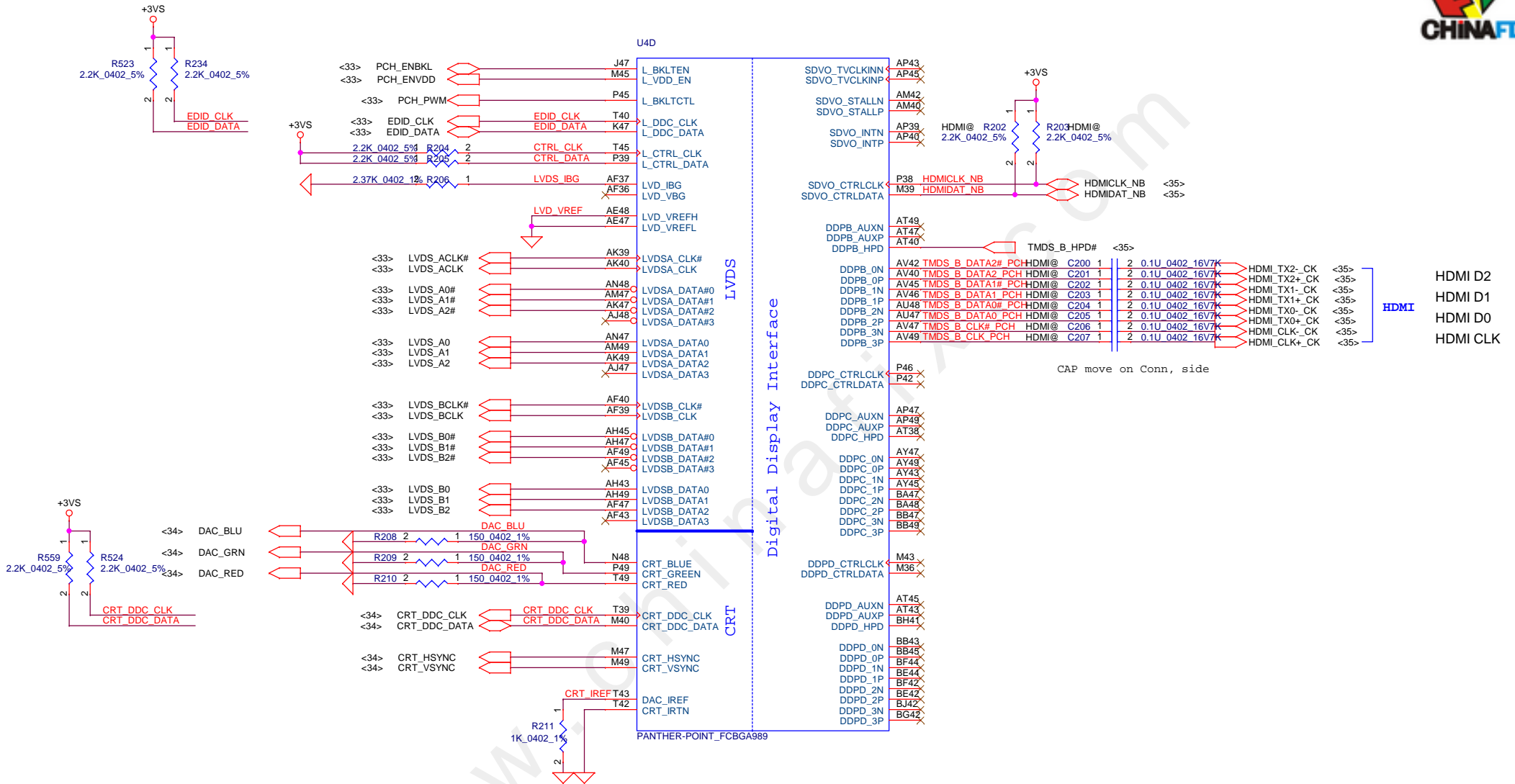
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Title <b>PCH (2/9) PCIE, SMBUS, CLK</b>			Rev 1.0
Date: Wednesday, January 09, 2013			Sheet 15 of 62



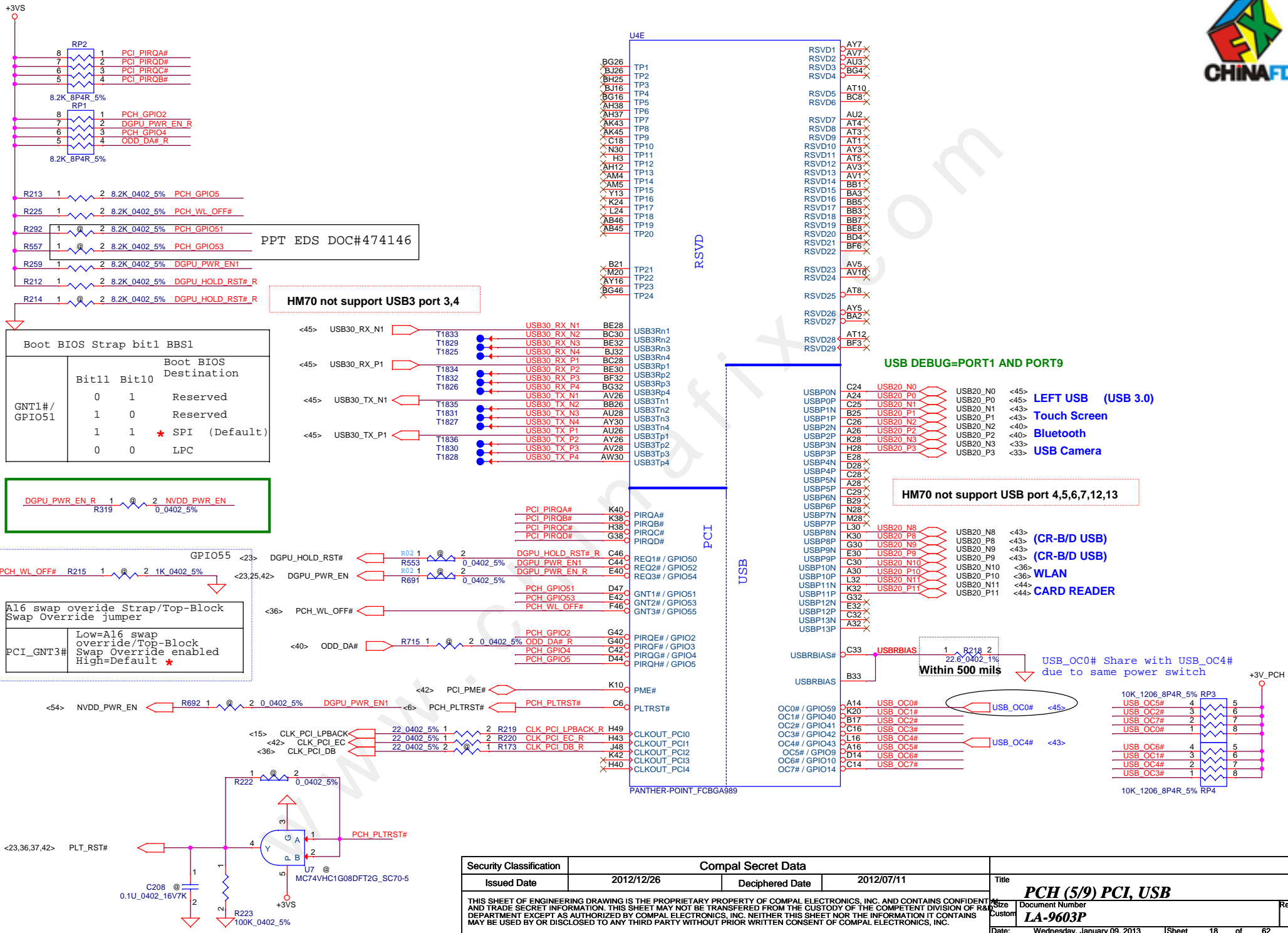


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PPT EDS DOC#474146

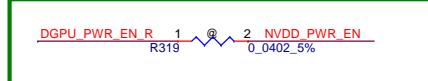
HM70 not support USB3 port 3,4

USB DEBUG=PORT1 AND PORT9

HM70 not support USB port 4,5,6,7,12,13

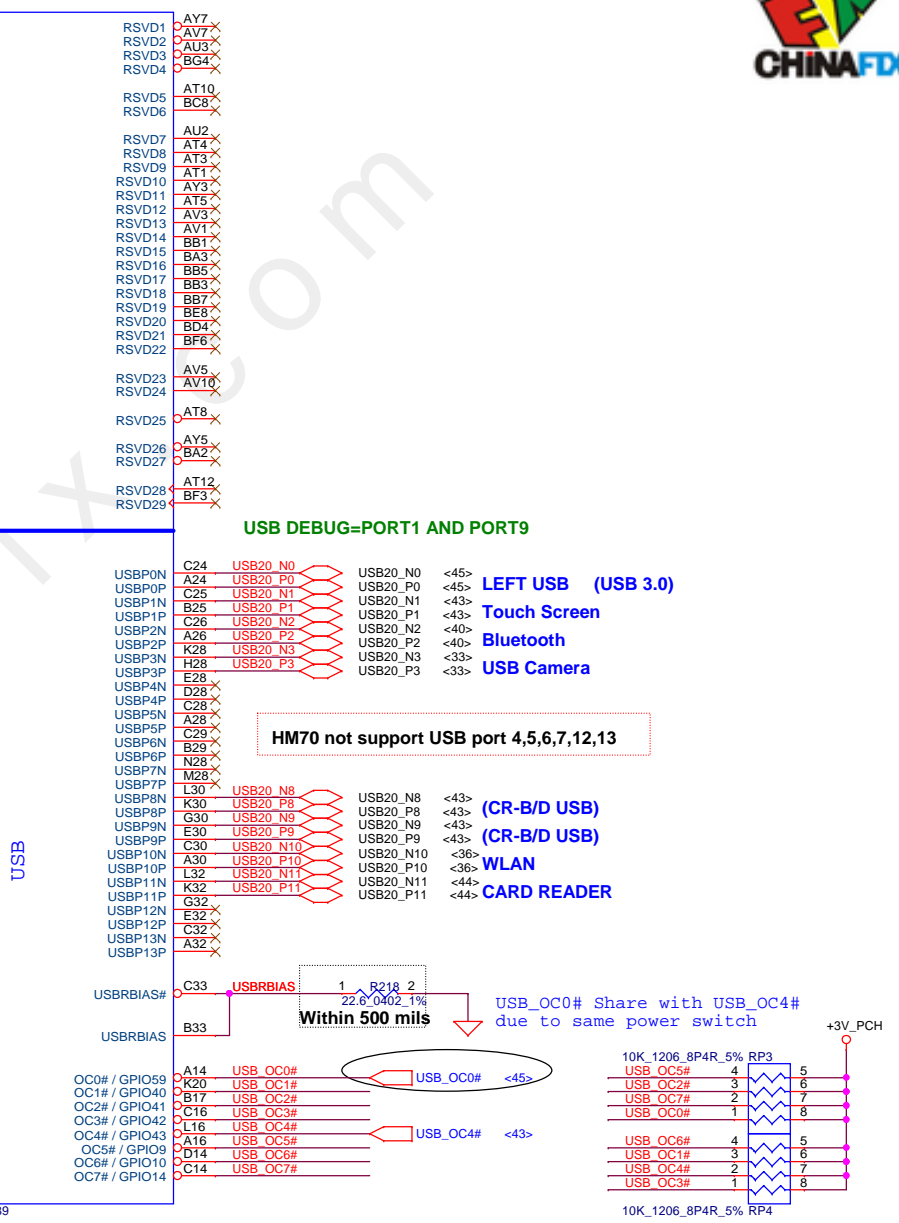
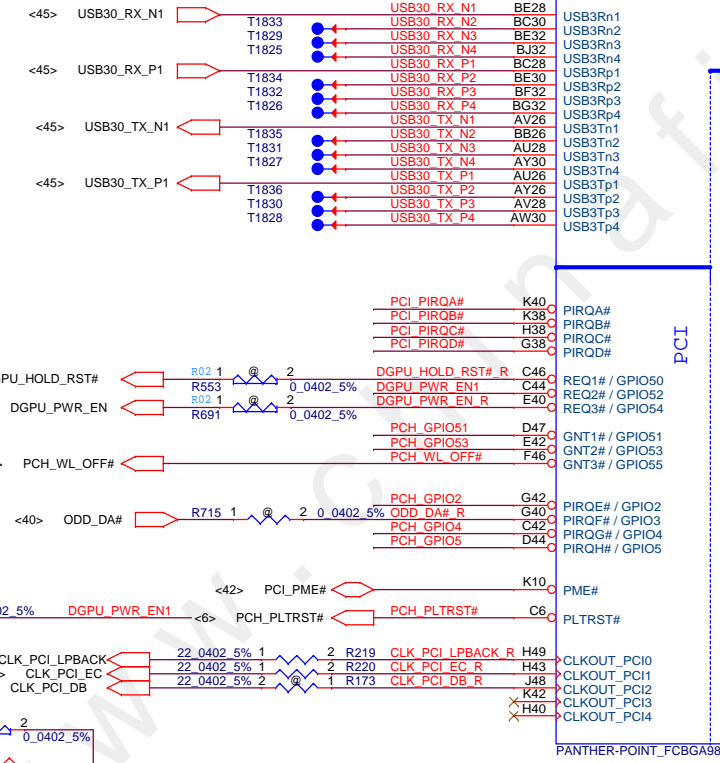
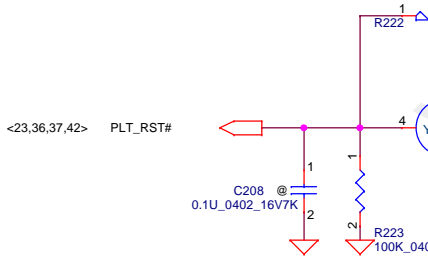
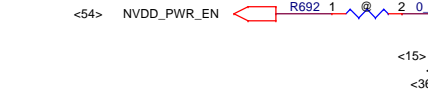
Boot BIOS Strap bit1 BBS1

Bit11	Bit10	Boot BIOS Destination
0	1	Reserved
1	0	Reserved
1	1	* SPI (Default)
0	0	LPC



A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled	High=Default *
0	1	0
1	0	1

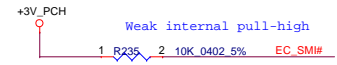


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PCH_GPIO69	Function
0	HM76 by PCH
1	HM70 by PCH

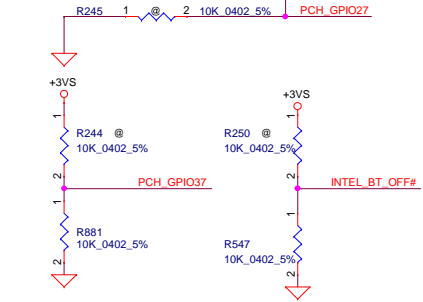
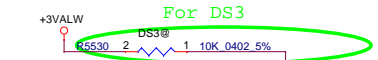
PCH_GPIO70	Function
0	UMA
1	N14P-GV2



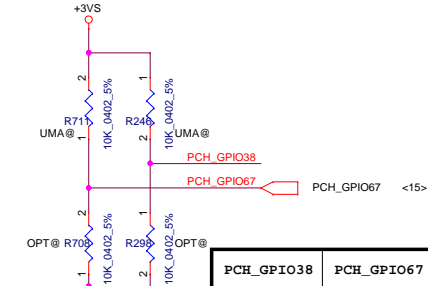
**GPIO28**  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
\* H : On-Die voltage regulator enable  
L : On-Die PLL Voltage Regulator disable

\* Deep S4,S5 wake event signal  
RTC alarm,Power BTN,GPIO27

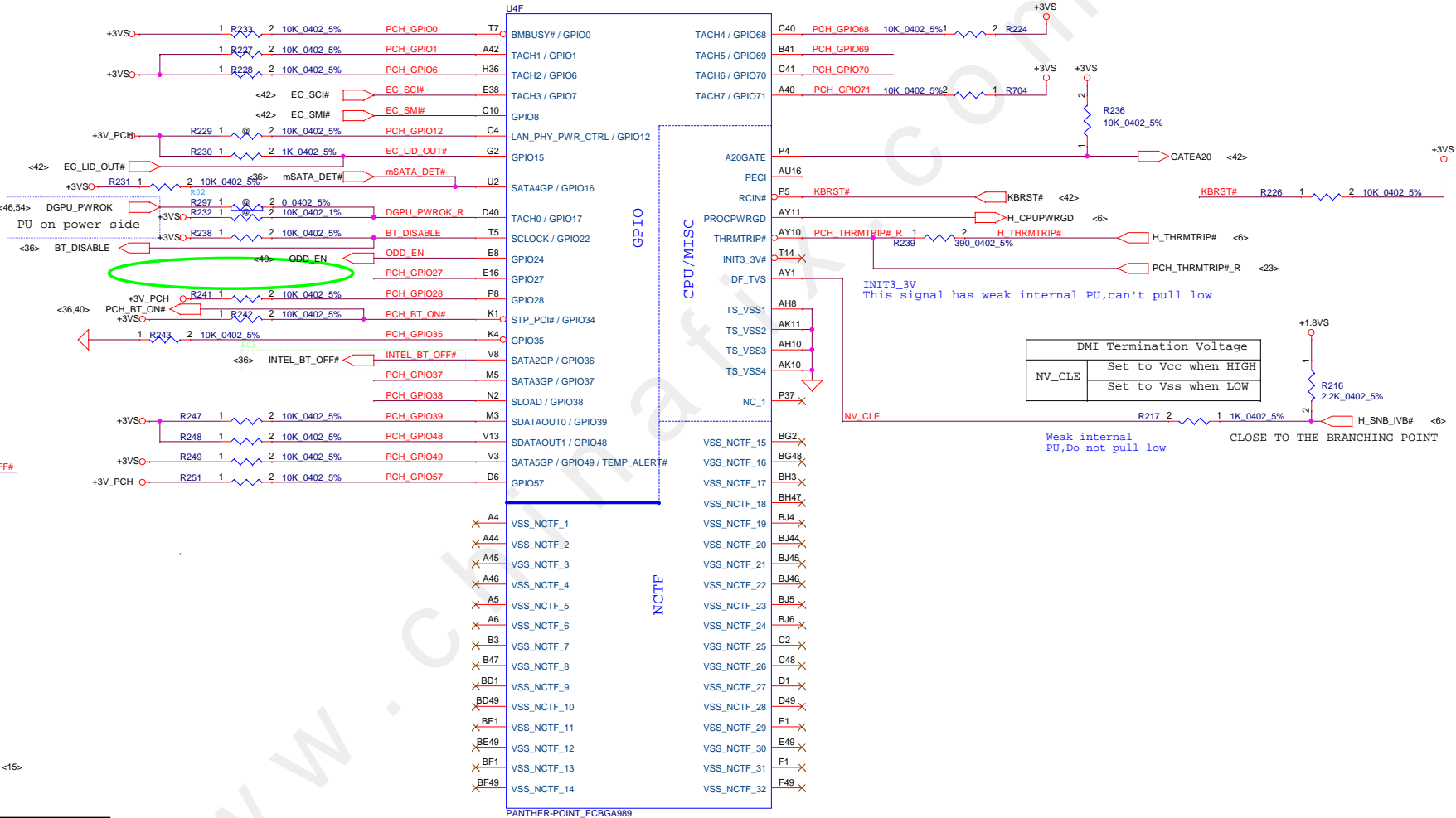
PCH\_GPIO27 (Have internal Pull-High)  
Deep S4,S5 wake event signal



BIOS Request SKU ID



PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
1	1	UMA



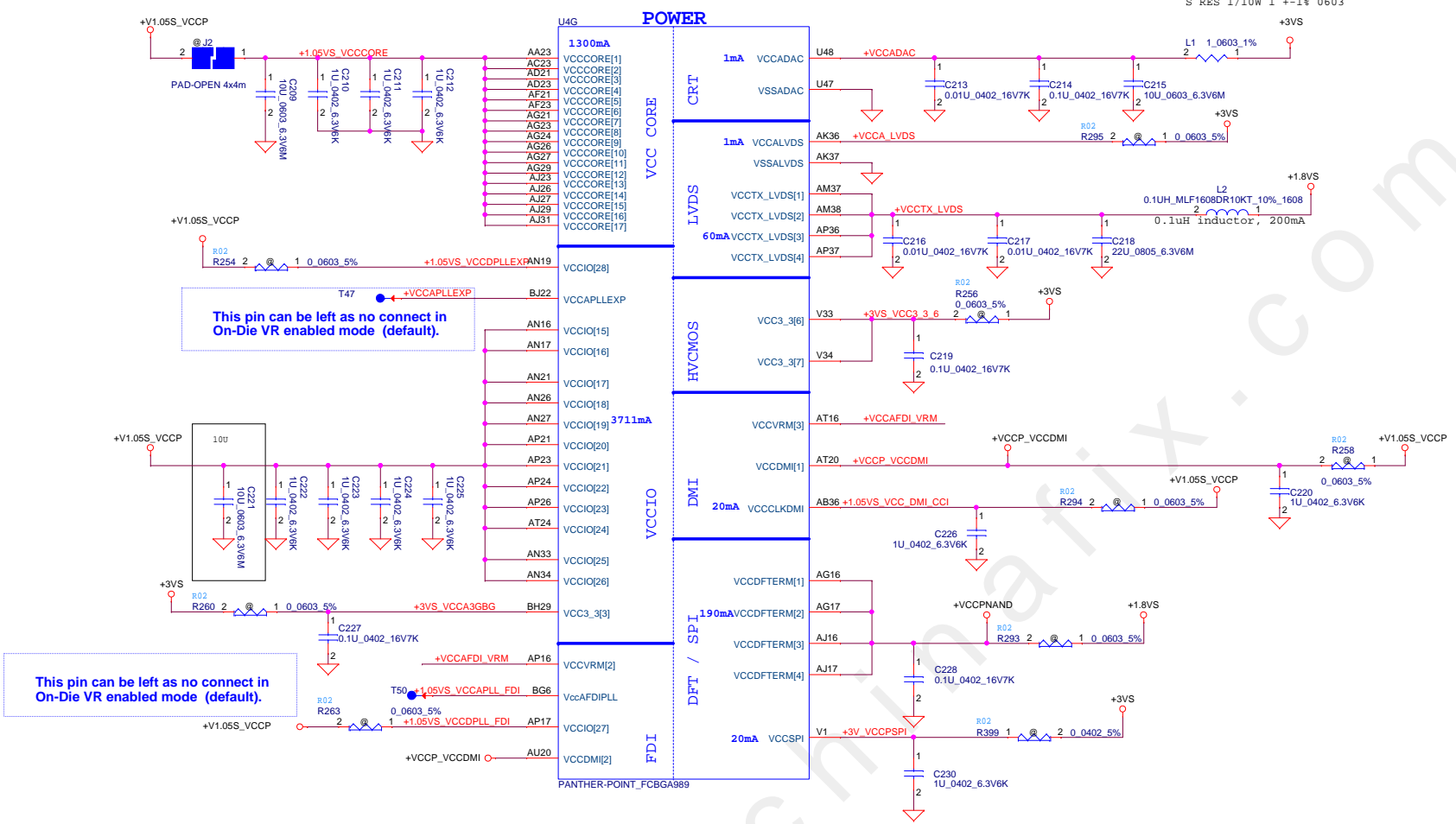
DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

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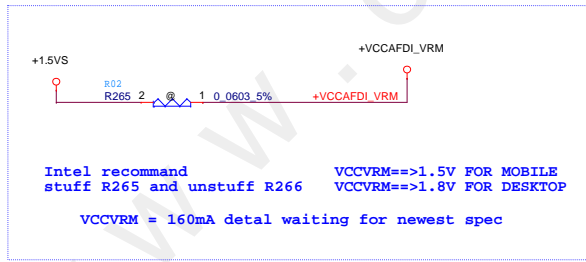
**PCH Power Rail Table**  
Refer to CPU EDS R1.5

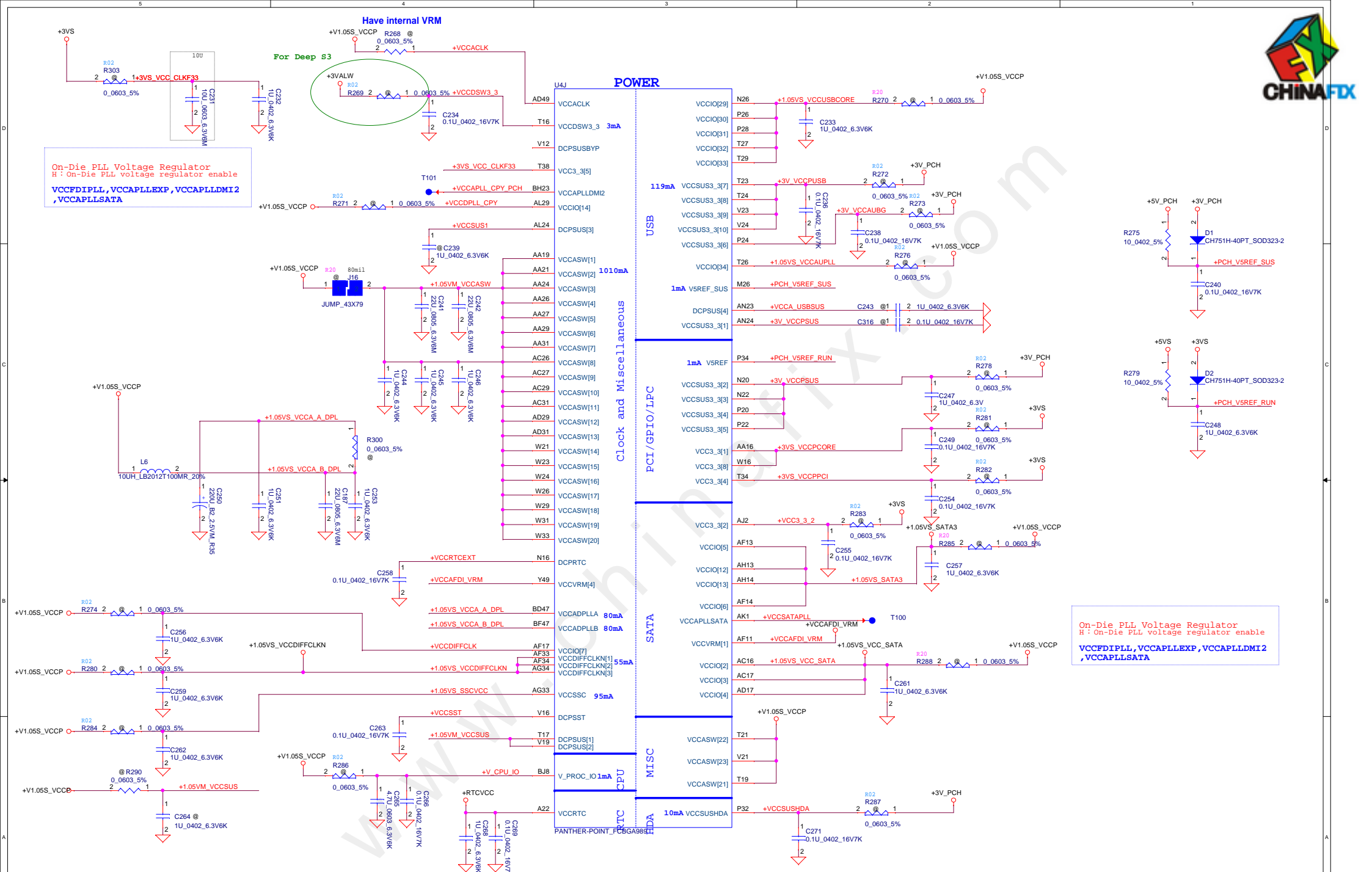
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



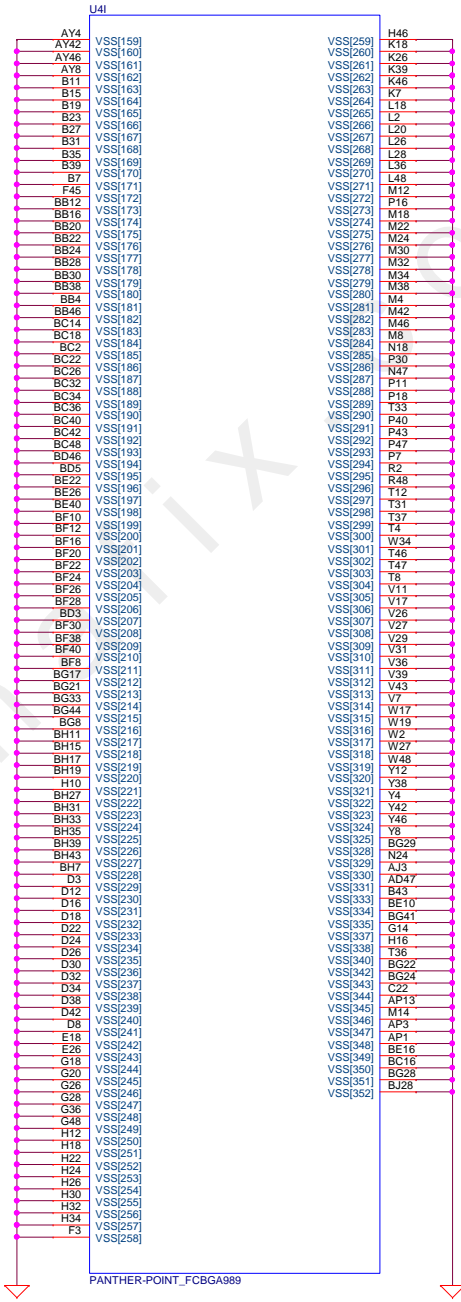
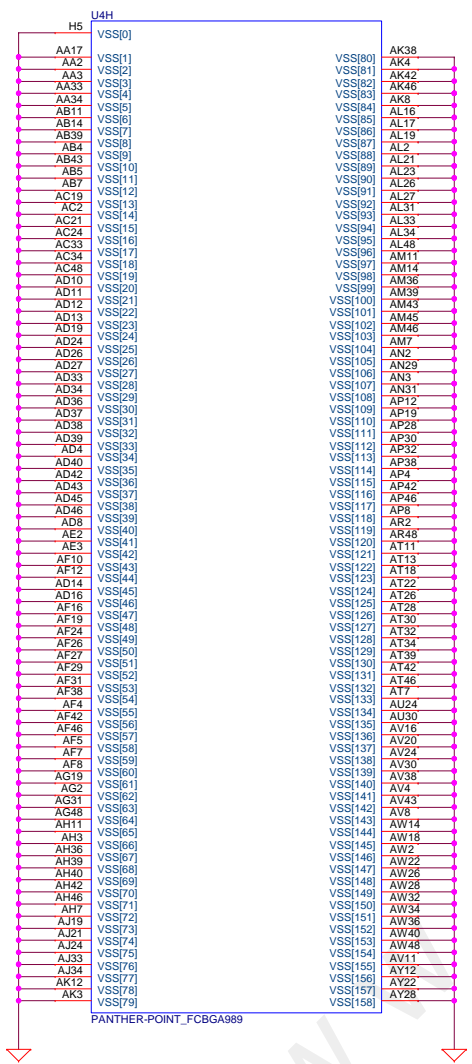
This pin can be left as no connect in On-Die VR enabled mode (default).

This pin can be left as no connect in On-Die VR enabled mode (default).





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			<b>Rev</b> 1.0
			<b>Date:</b> Wednesday, January 09, 2013   <b>Sheet</b> 21 of 62



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				Rev 1.0

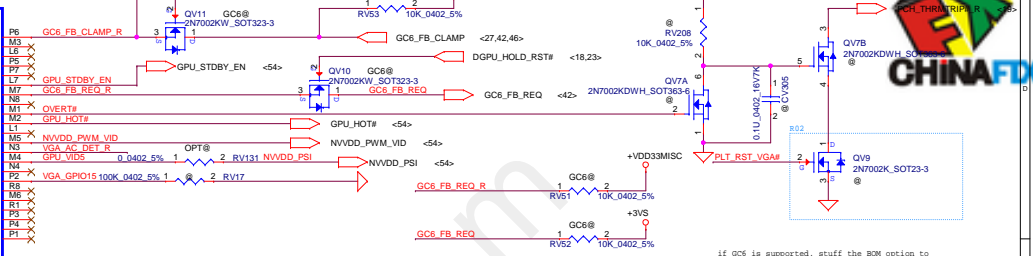
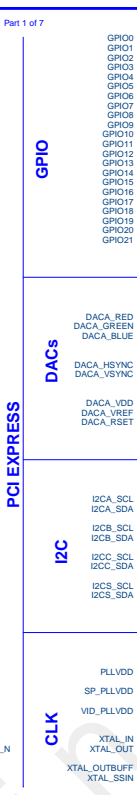


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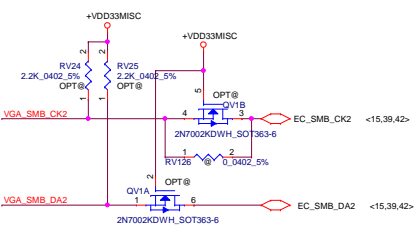
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- PCIE\_CTX\_GRX\_P2 AP14 PEX\_RX2
- PCIE\_CTX\_GRX\_N2 AP15 PEX\_RX2\_N
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- PCIE\_CTX\_GRX\_N5 AP17 PEX\_RX5\_N
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- PCIE\_CTX\_GRX\_N6 AN18 PEX\_RX6\_N
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- PCIE\_CTX\_GRX\_P15 AN27 PEX\_RX15
- PCIE\_CTX\_GRX\_N15 AN27 PEX\_RX15\_N

- PCIE\_CRX\_GTX\_P0 CV16 2 2.22u 0.402 6.3V/K OPT@ PCIE\_CRX\_C\_GTX\_P0 AK14 PEX\_TX0
- PCIE\_CRX\_GTX\_N0 CV7 2 2.22u 0.402 6.3V/K OPT@ PCIE\_CRX\_C\_GTX\_N0 AJ14 PEX\_TX0\_N
- PCIE\_CRX\_GTX\_P1 CV8 2 2.22u 0.402 6.3V/K OPT@ PCIE\_CRX\_C\_GTX\_P1 AH14 PEX\_TX1
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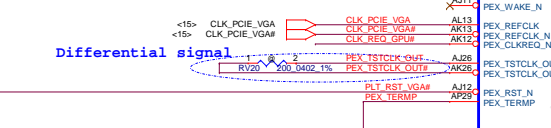
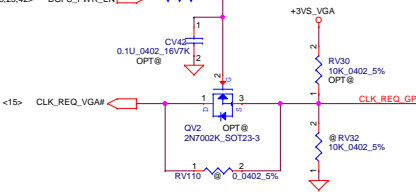
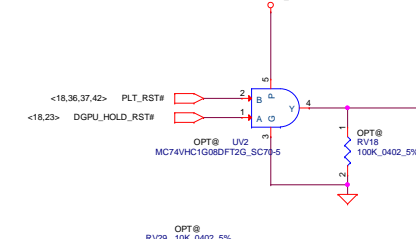


For N13P-GS Reserve for GTGE leakage issue

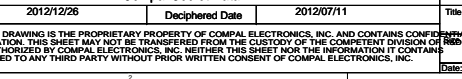
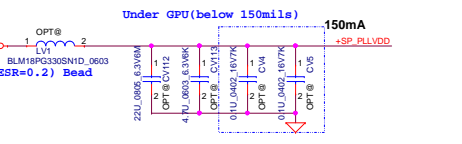
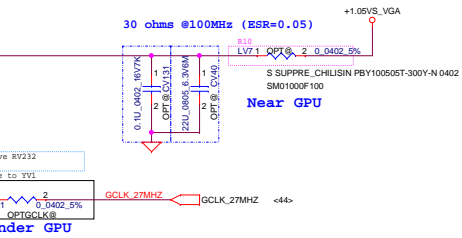
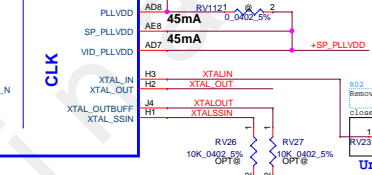
if GC6 is supported, stuff the ROW option to pull high to 3.3v system power. If not, stuff the ROW option to pull high to NV7V1



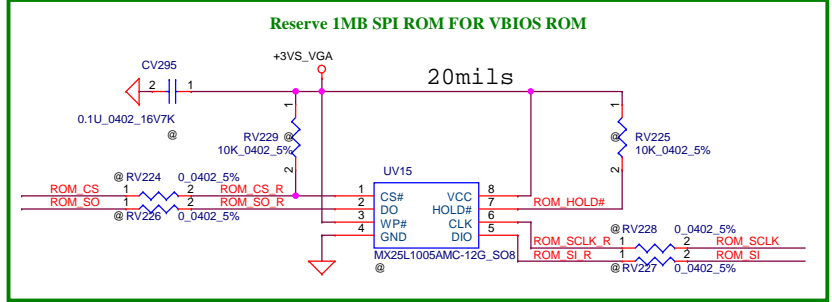
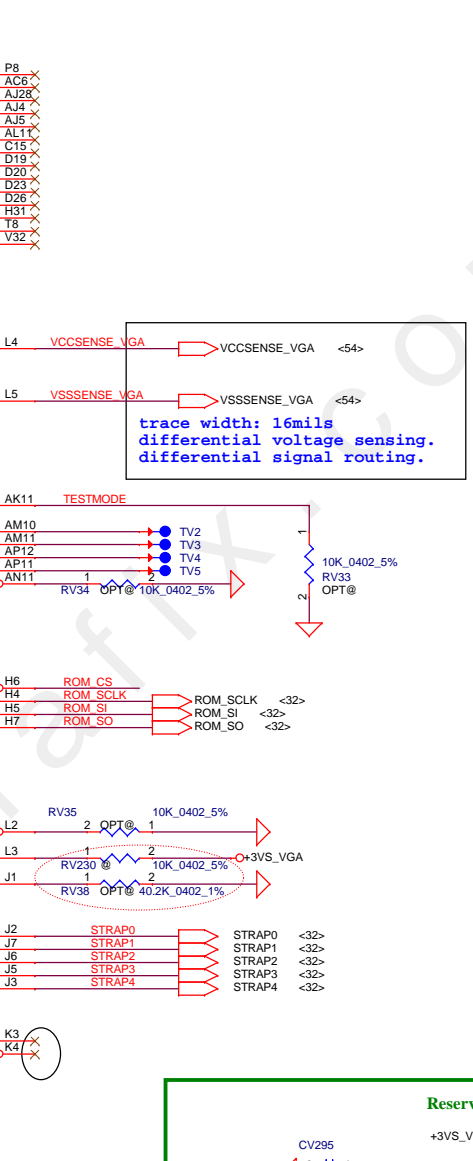
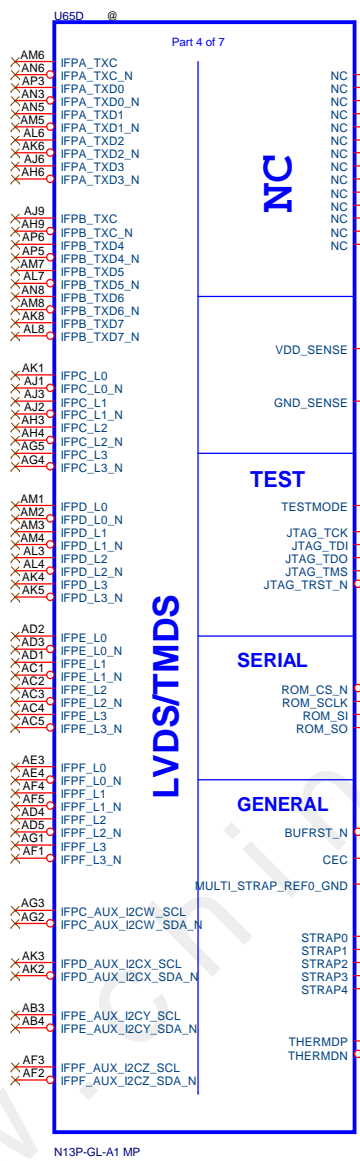
PU AT EC SIDE, +3VS AND 4.7K



Differential signal

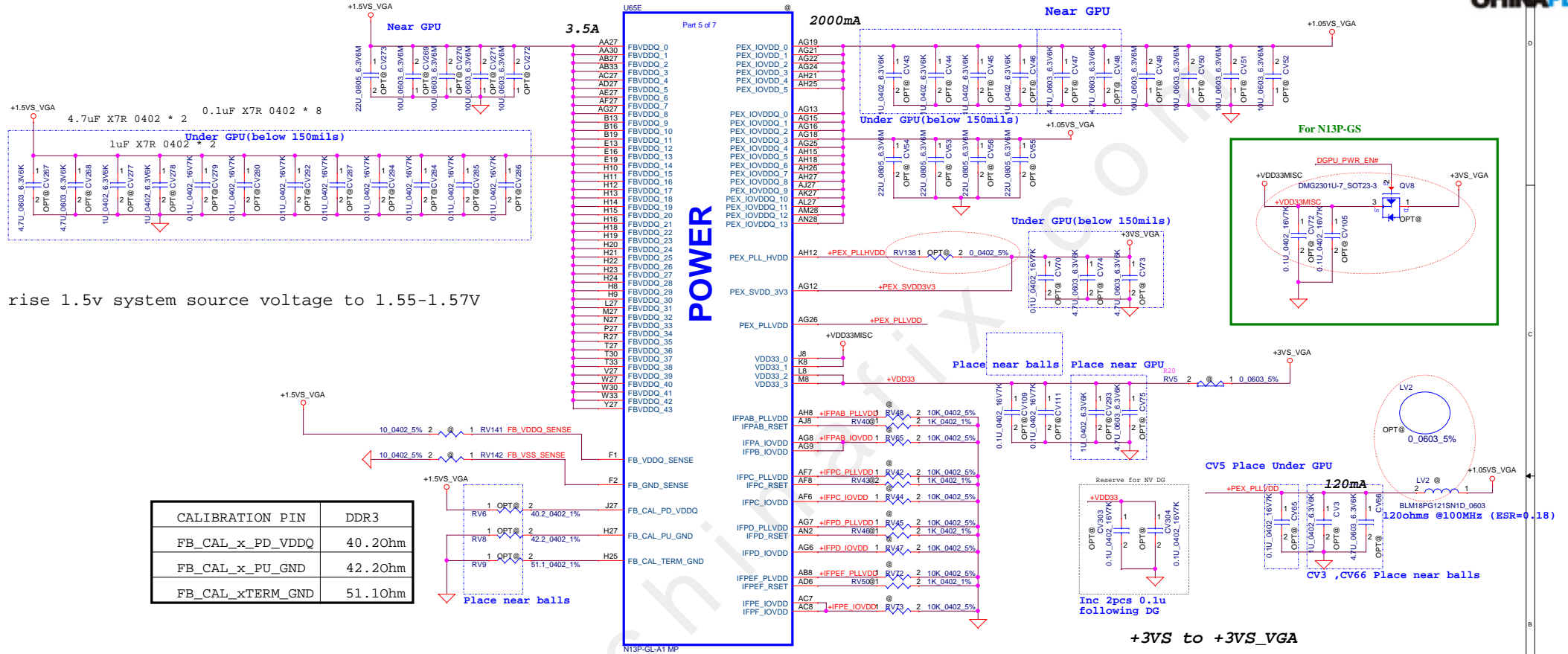


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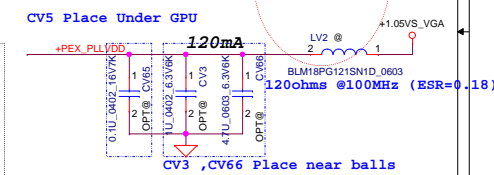
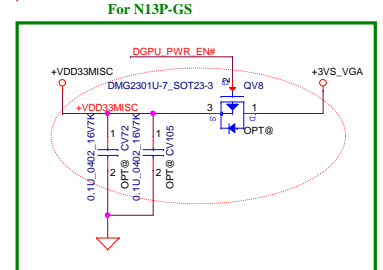
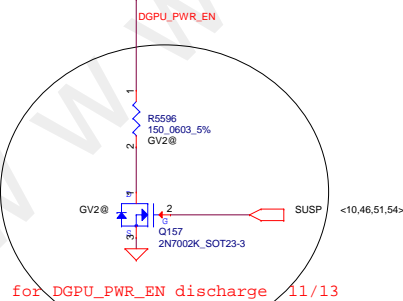
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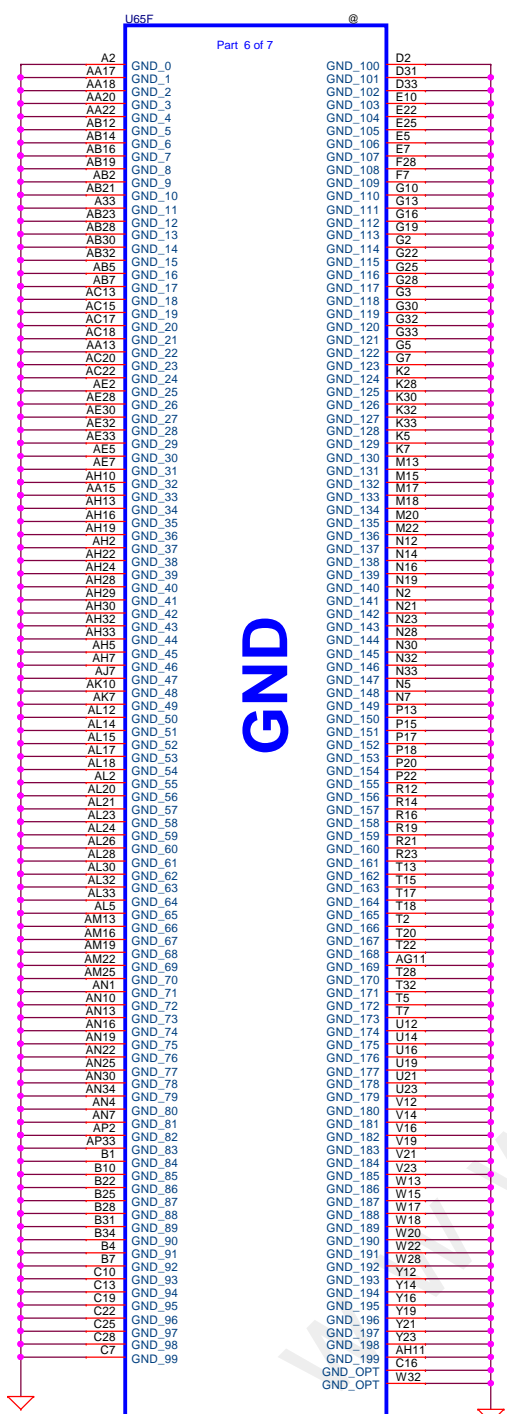


rise 1.5v system source voltage to 1.55-1.57V

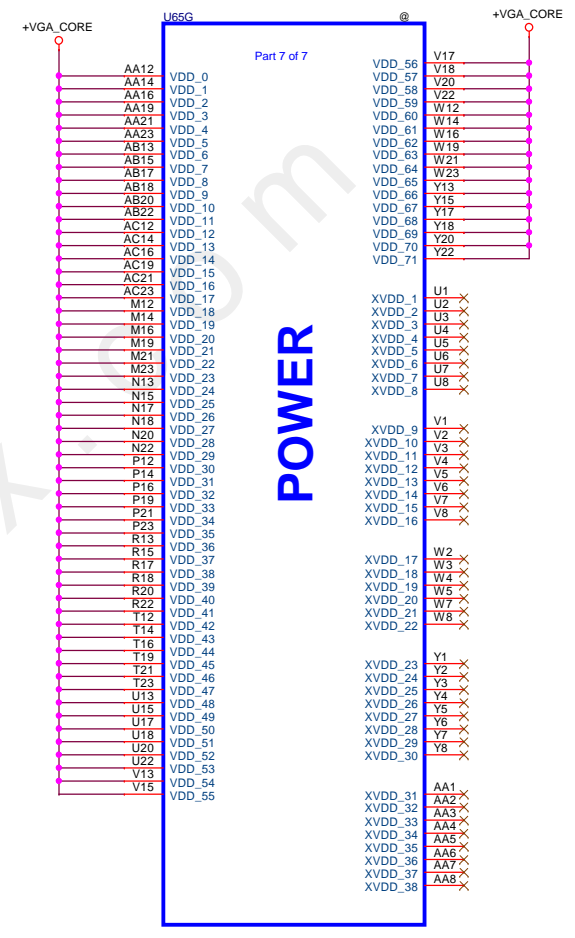
CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.20ohm
FB_CAL_x_PU_GND	42.20ohm
FB_CAL_x_TERM_GND	51.10ohm



+3VS to +3VS\_VGA

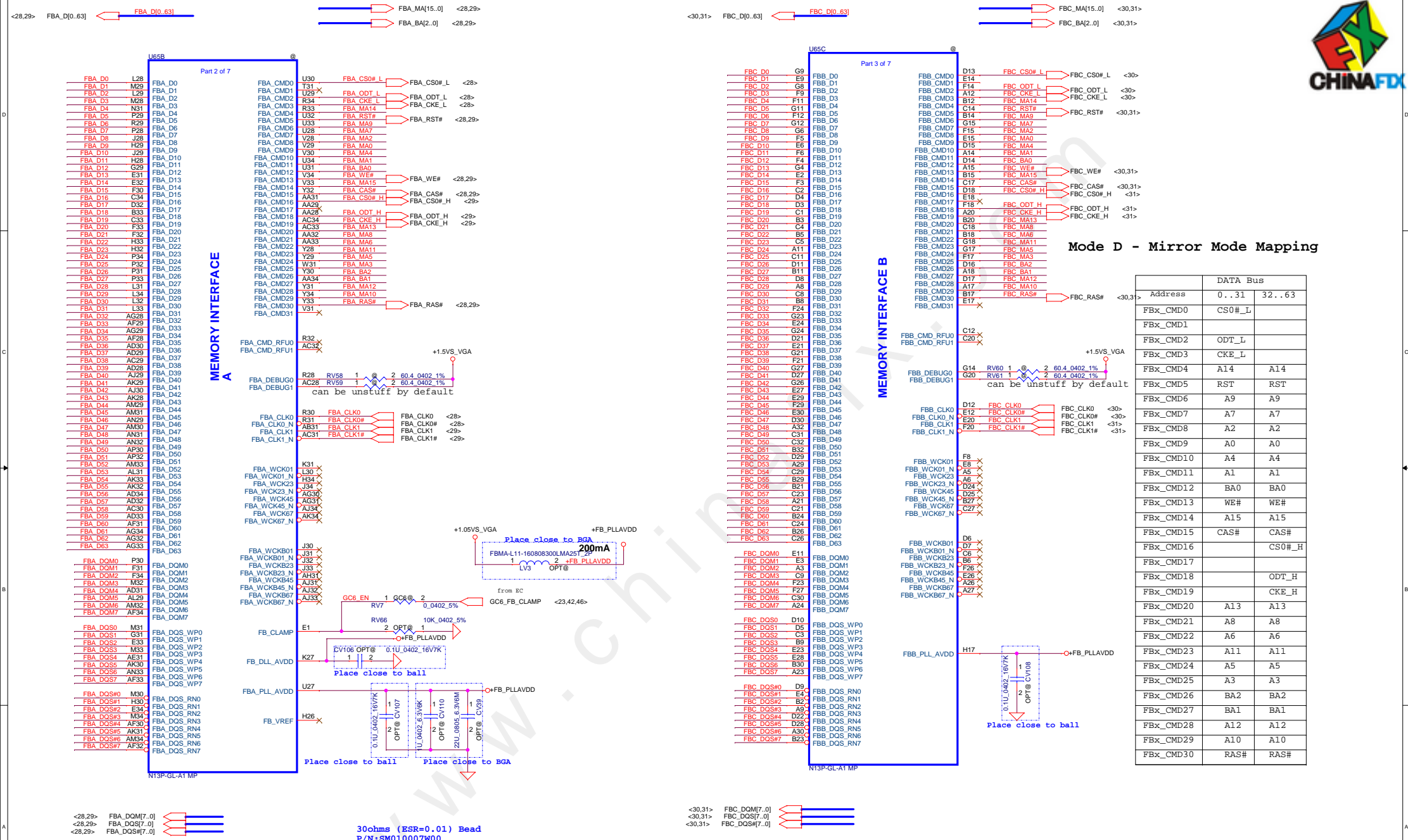


N13P-GL-A1 MP



N13P-GL-A1 MP

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Mode D - Mirror Mode Mapping

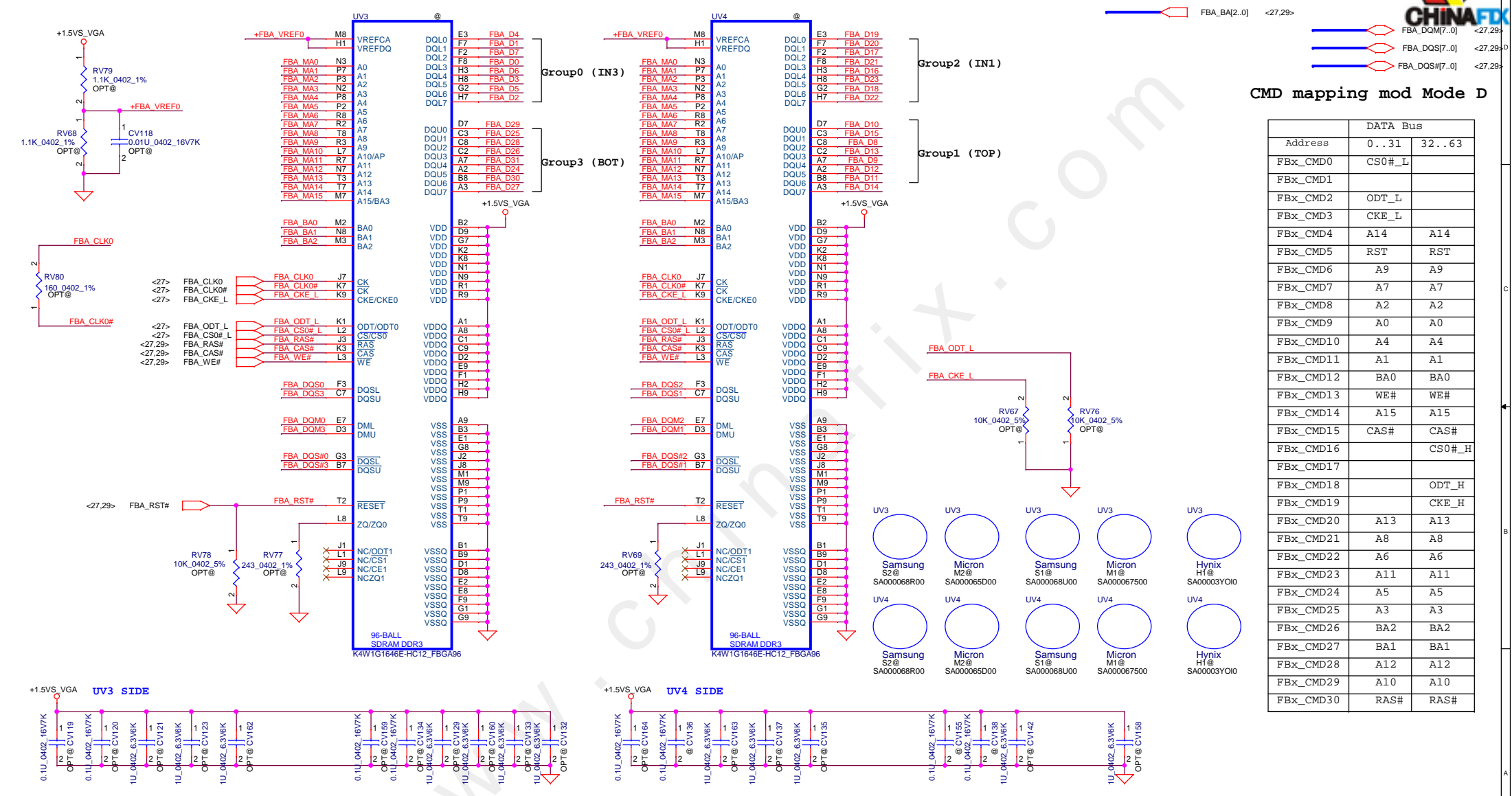
	Address	DATA Bus
FBx_CMD0	0..31	32..63
FBx_CMD1	CS0#_L	
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CS0#_H	
FBx_CMD17		
FBx_CMD18		
FBx_CMD19	ODT_H	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

<28..29> FBA\_DQM[7..0]  
 <28..29> FBA\_DQS[7..0]  
 <28..29> FBA\_DQS#(7..0)

30ohms (ESR=0.01) Bead  
 P/N:SM10007W00



# Memory Partition A - Lower 32 bits



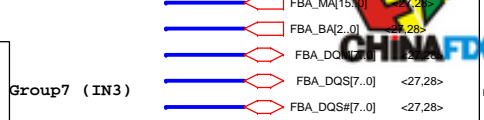
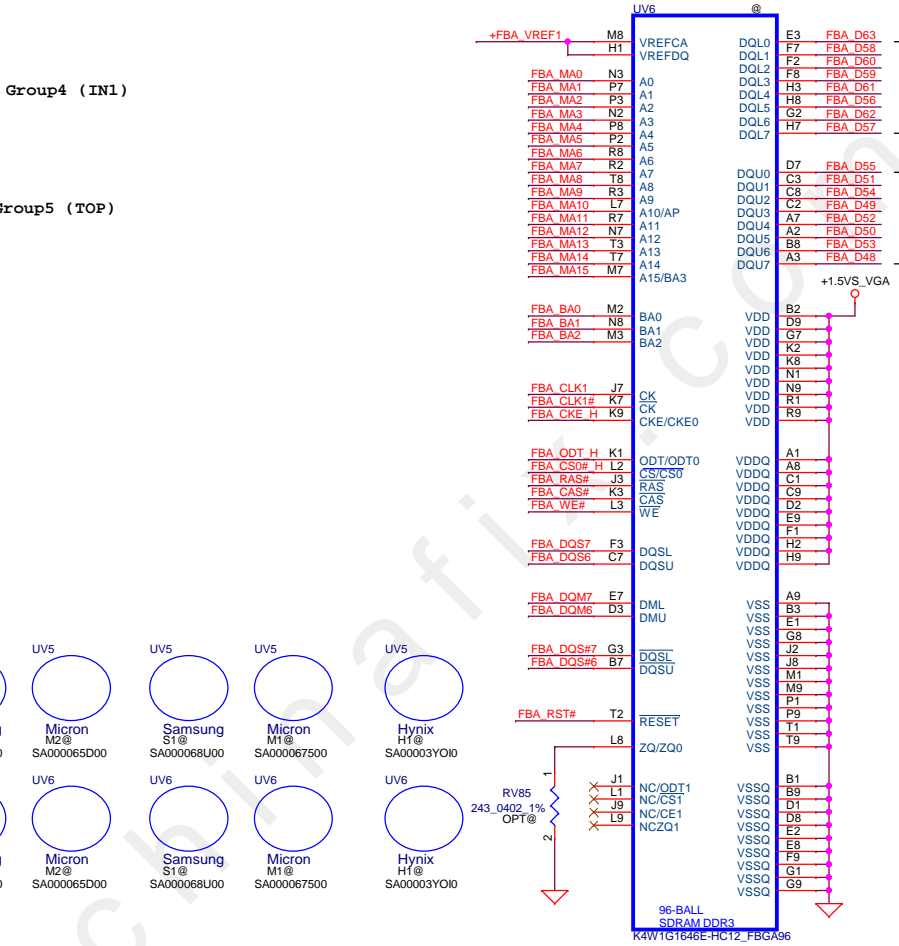
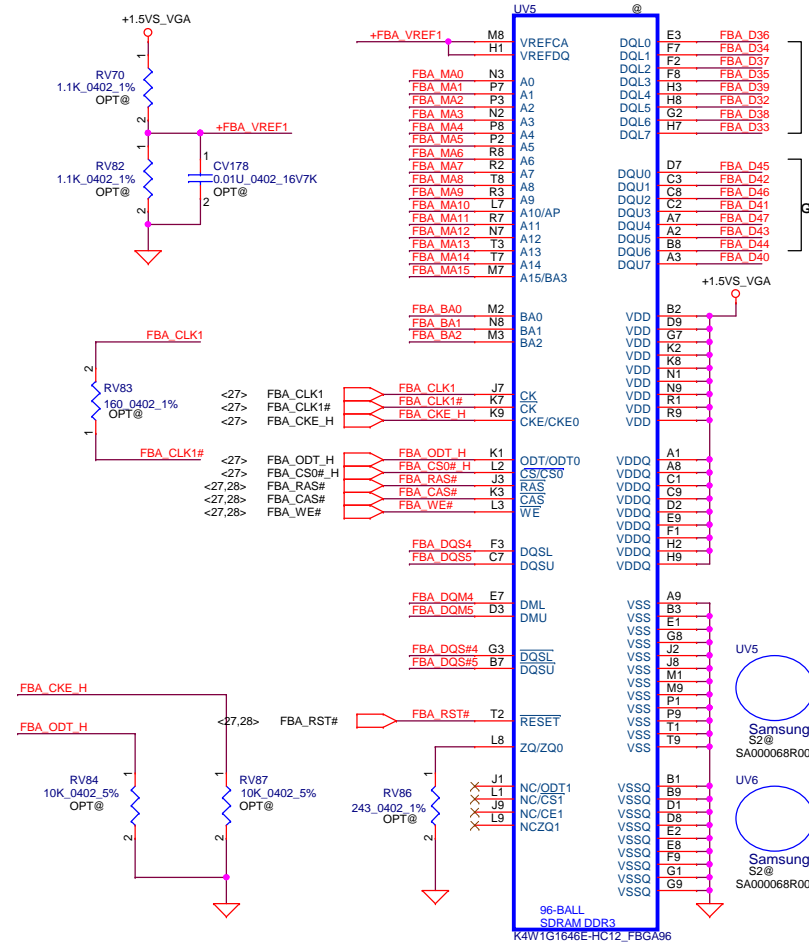
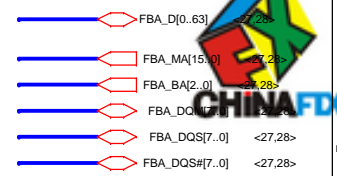
CMD mapping mod Mode D

Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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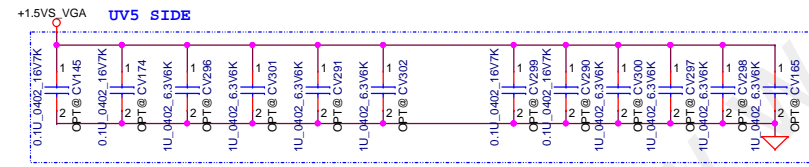


# Memory Partition A - Upper 32 bits



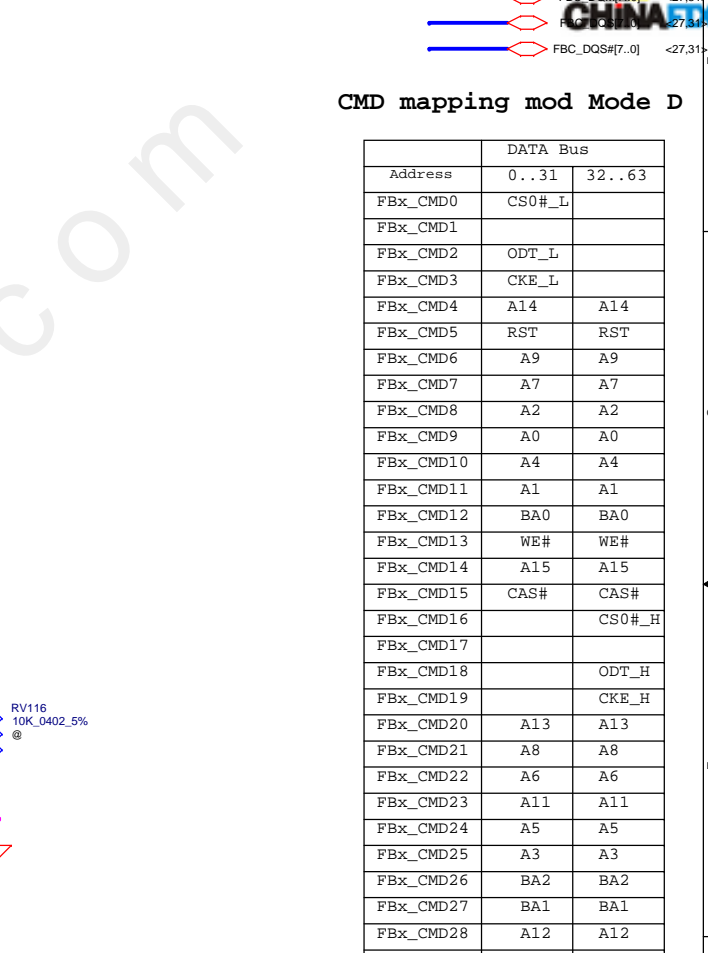
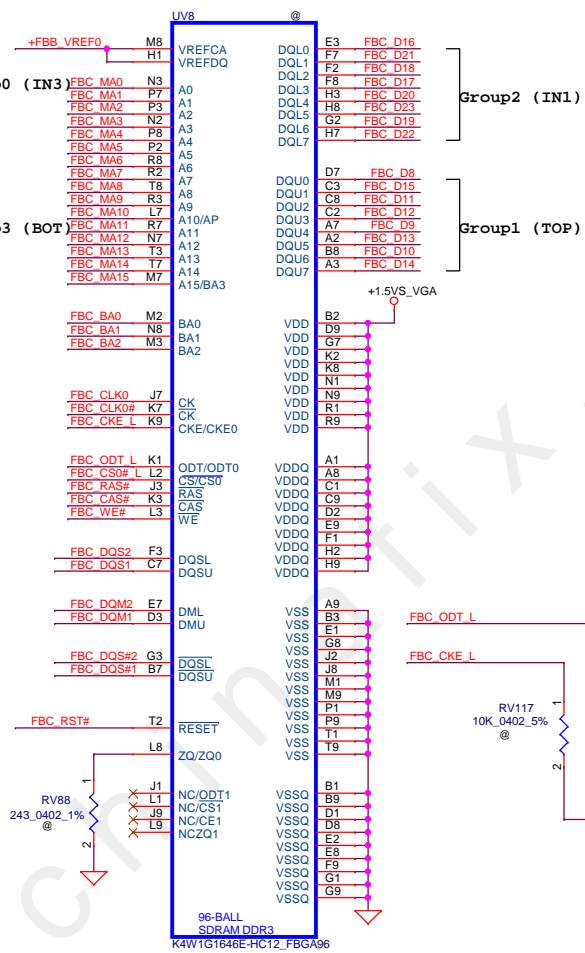
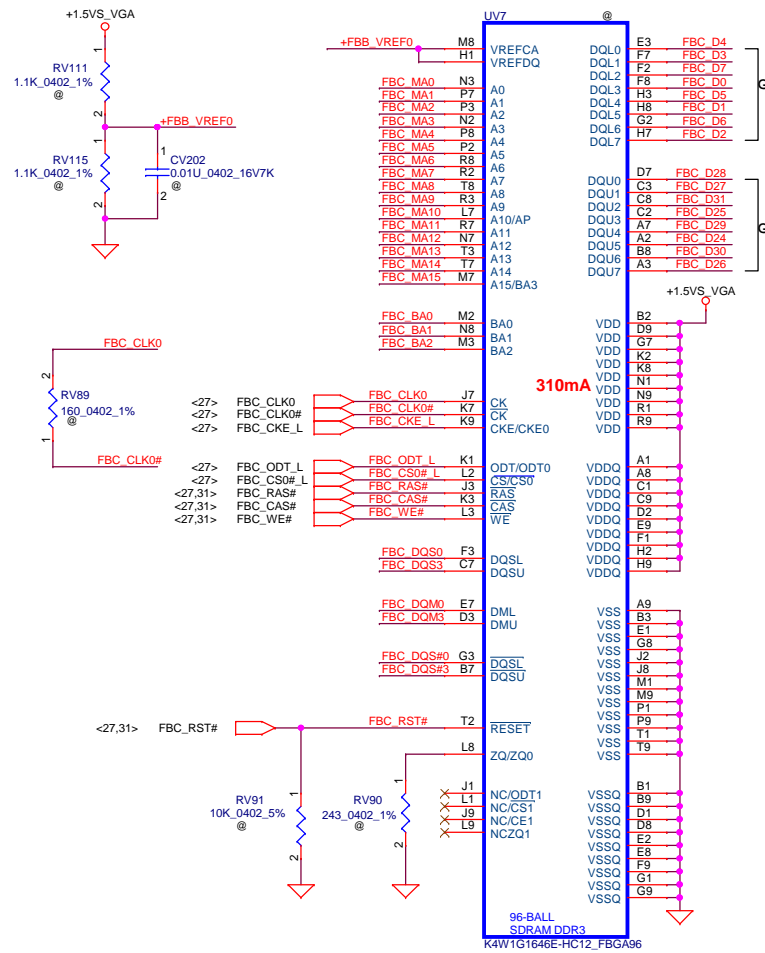
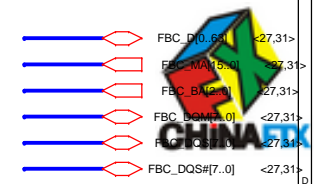
### CMD mapping mod Mode D

Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



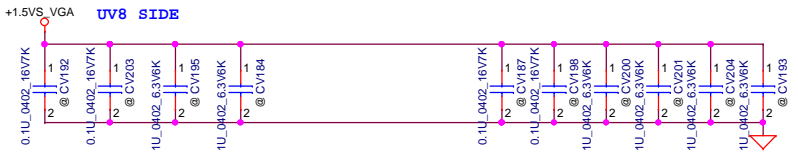
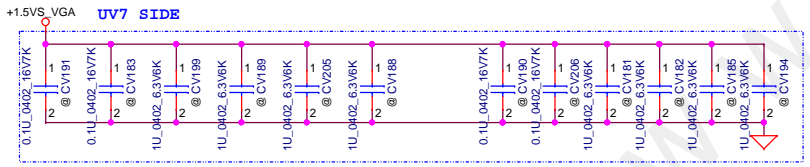
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# Memory Partition C - Lower 32 bits

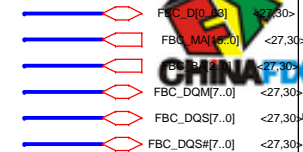


CMD mapping mod Mode D

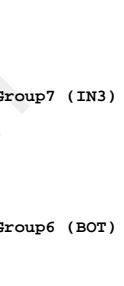
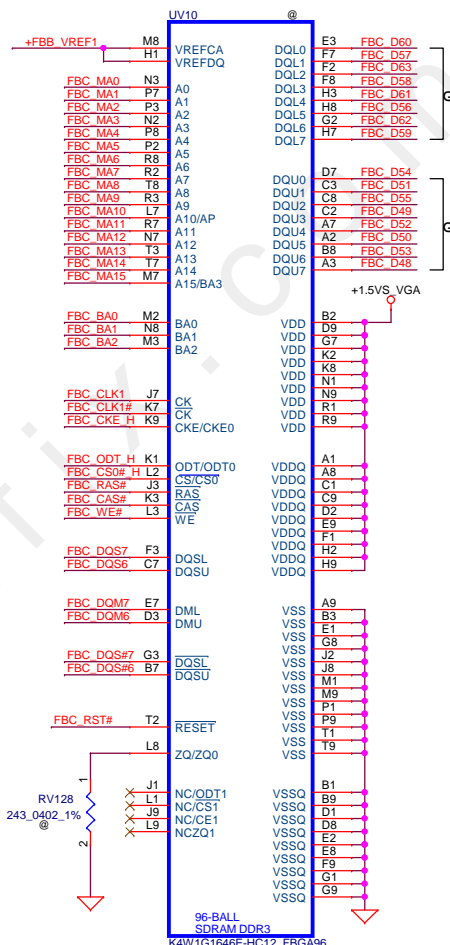
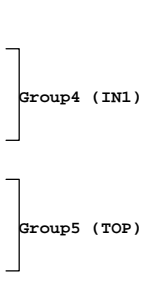
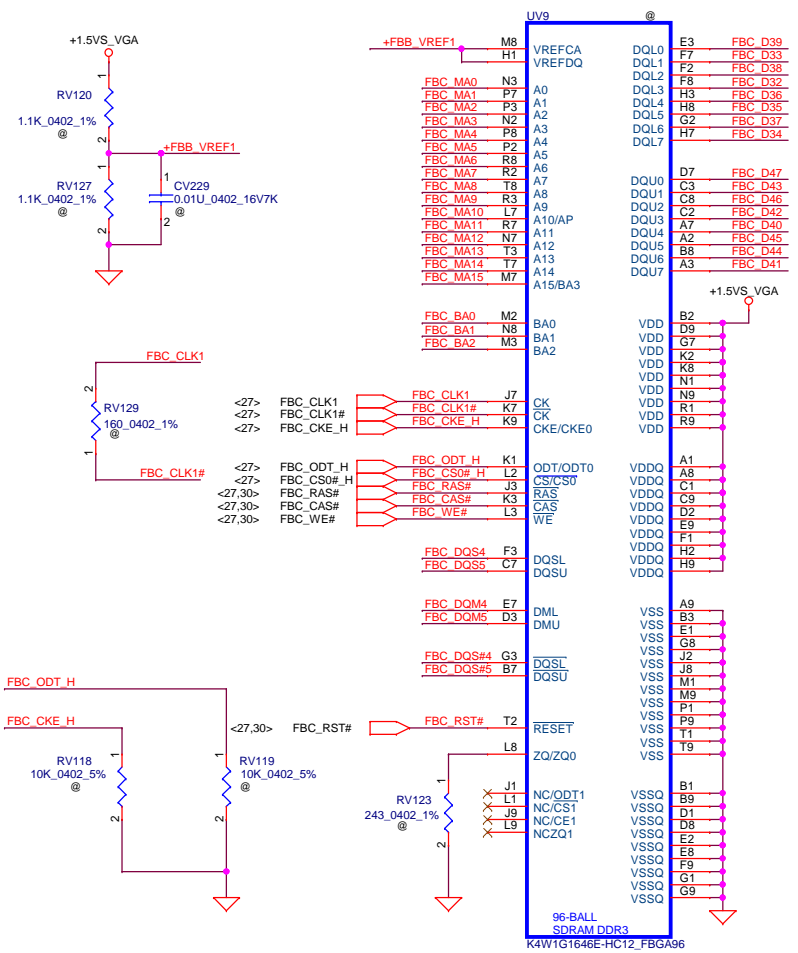
Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18	ODT_H	
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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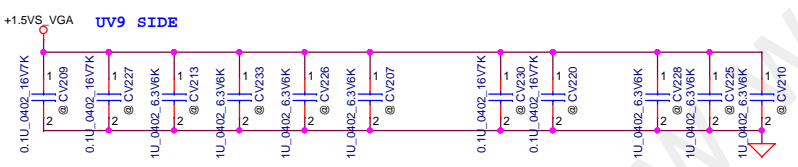


# Memory Partition C - Upper 32 bits

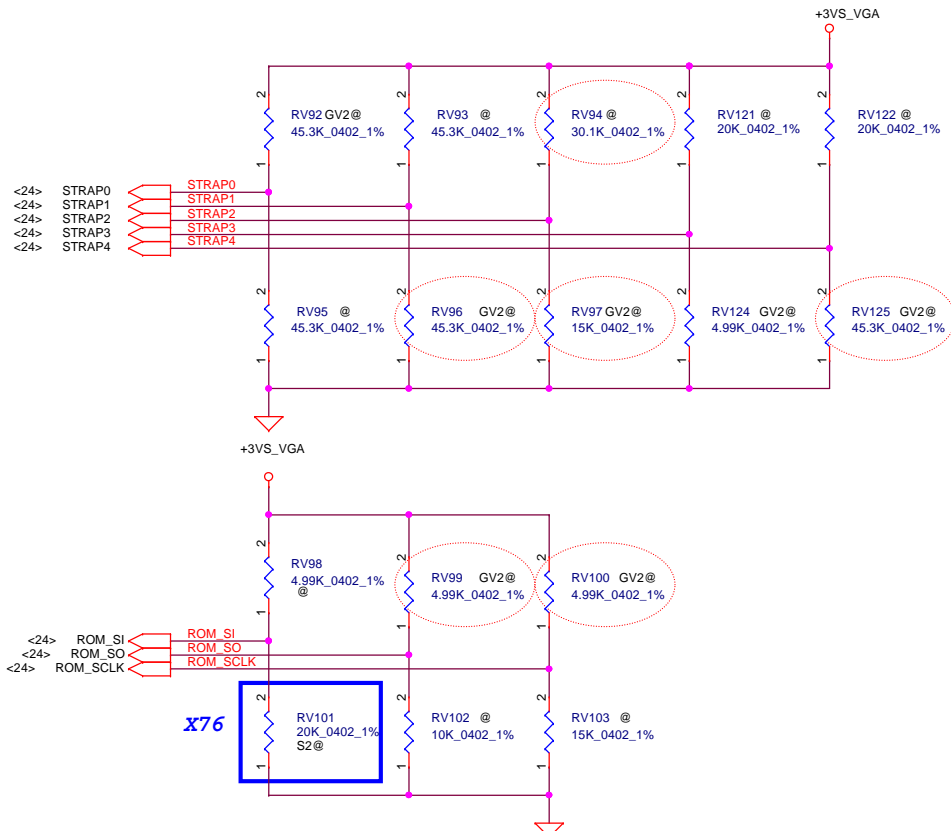


## CMD mapping mod Mode D

Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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				N13X-VRAM C Upper	
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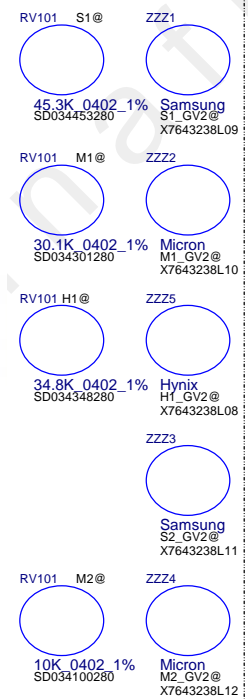
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Vendor	VRAM Structure
Samsung 2G	S2@
Micron 2G	M2@
Samsung 1G	S1@
Micron 1G	M1@

Table 3. N14M-G5/LP and N14P-GV2 DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production Candidate
				MT41J128M16JT-107G:K	900	1150	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-N0C	1000	N/A	Production Candidate
				H5TQ2G63DFR-11C	900	N/A	Production Candidate
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production Candidate
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production Candidate



SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

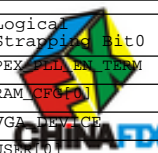
XCLK_417	
0	277MHz (Default)
1	Reserved

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

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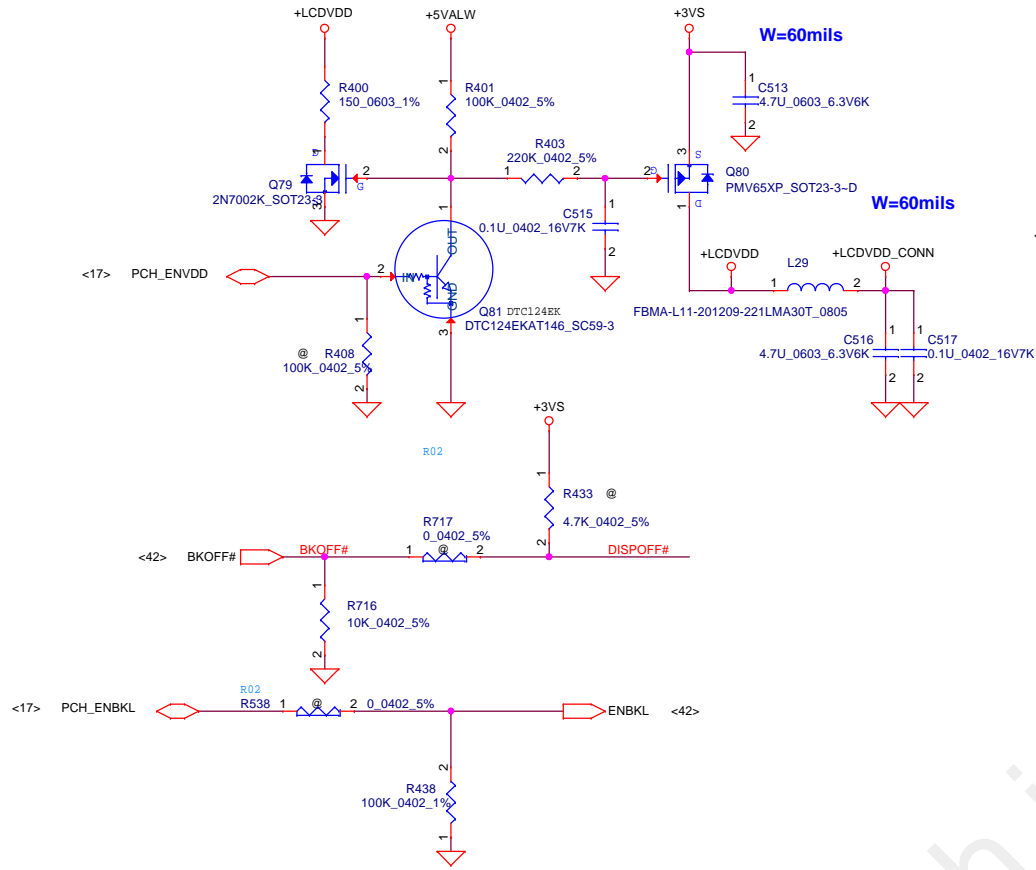
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Title	N13X MISC	
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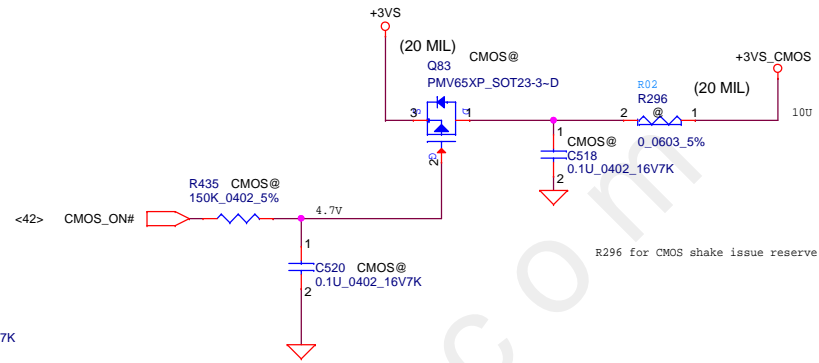




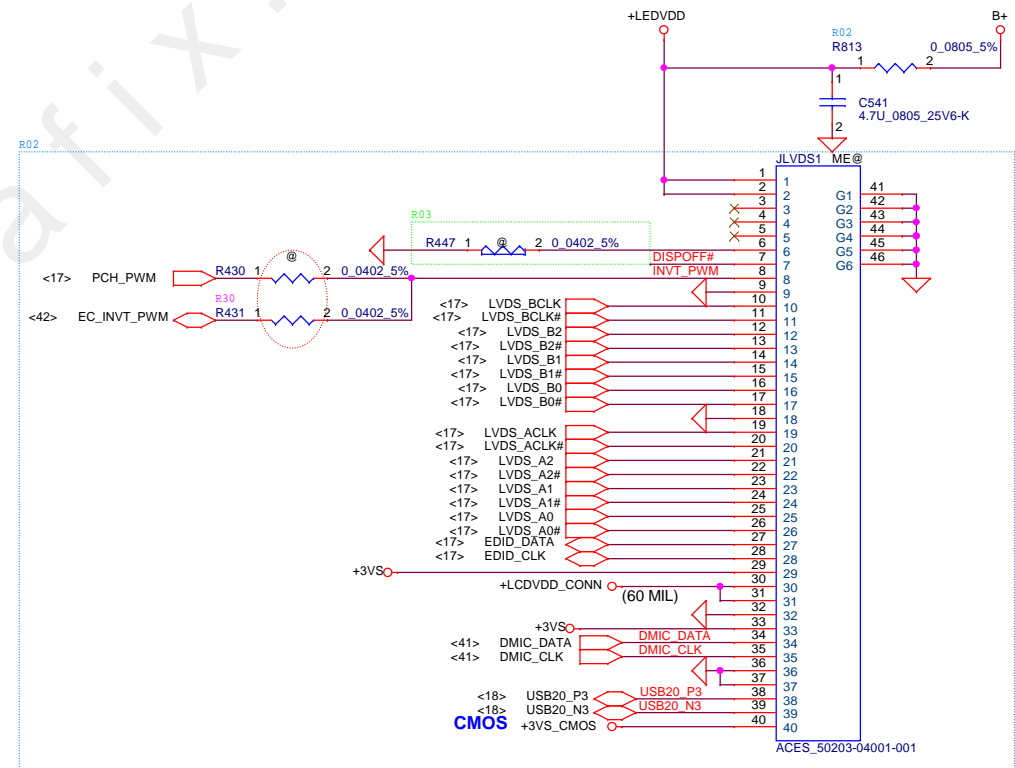
# LCD POWER CIRCUIT



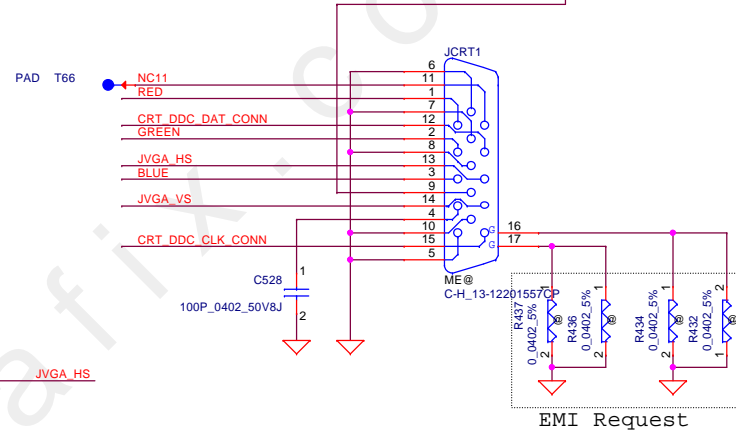
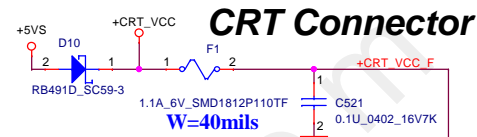
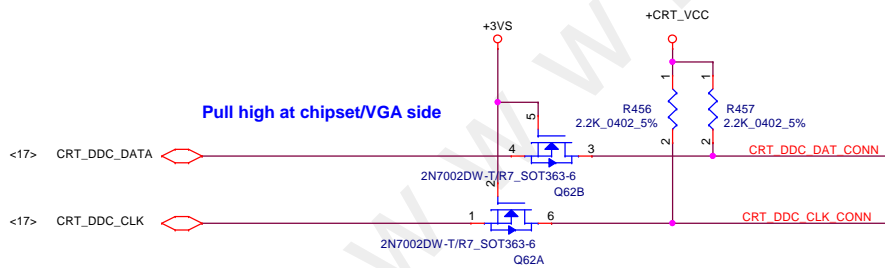
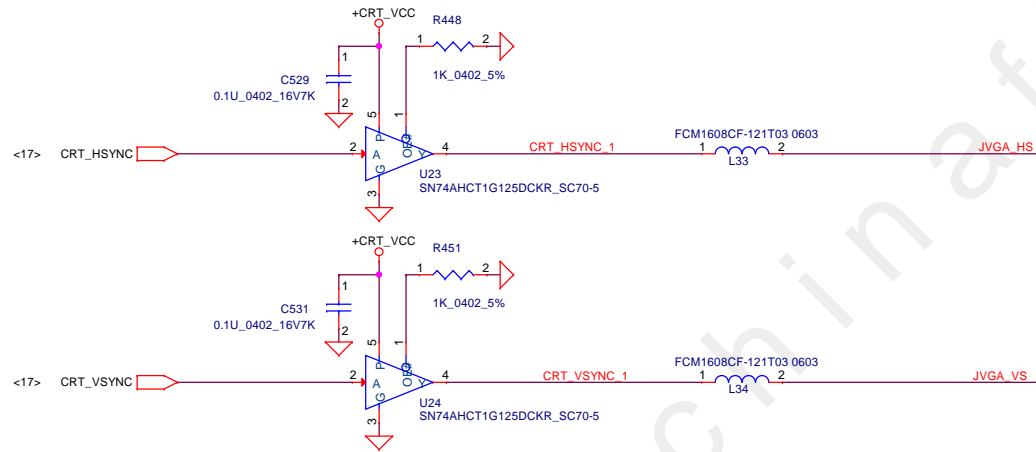
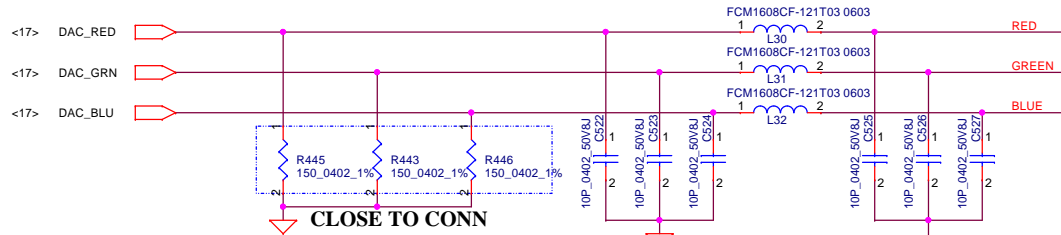
# CMOS Camera



# VGA LCD/PANEL BD. Conn.

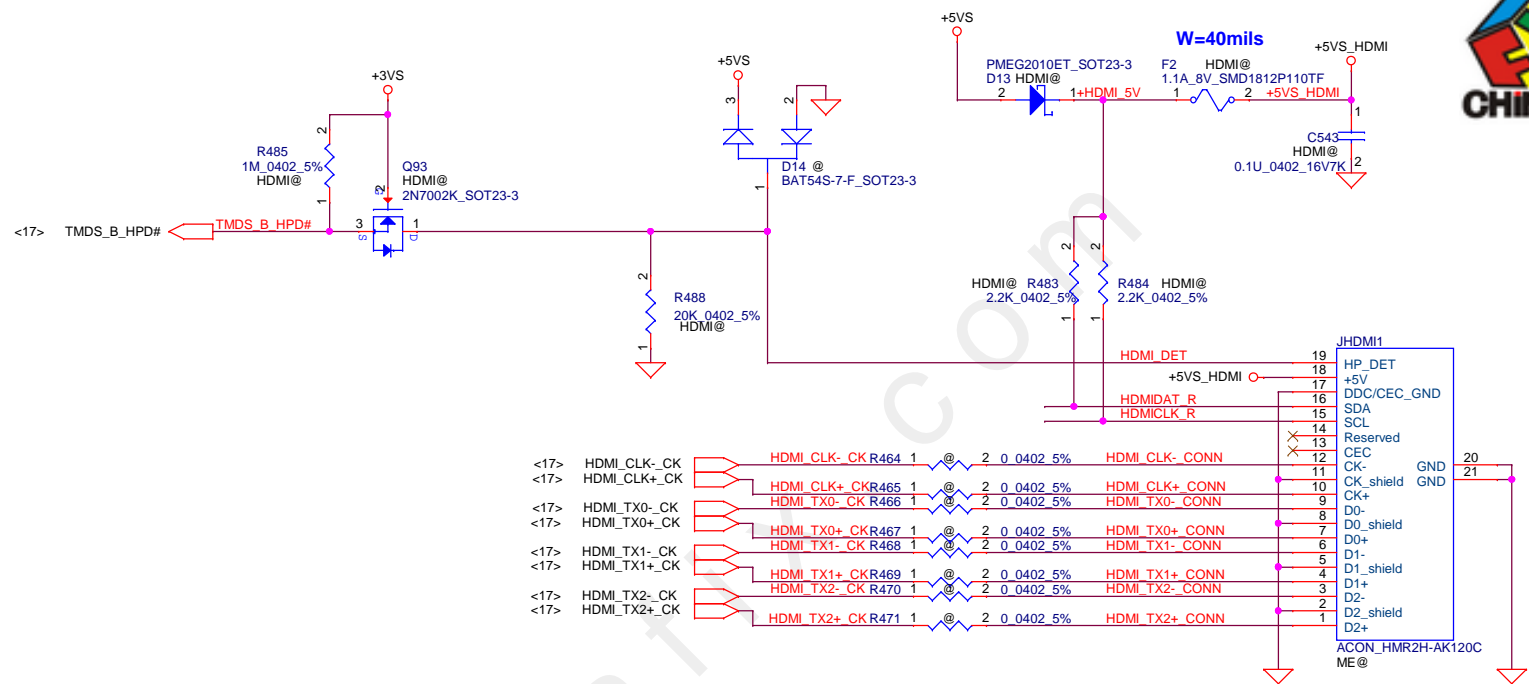


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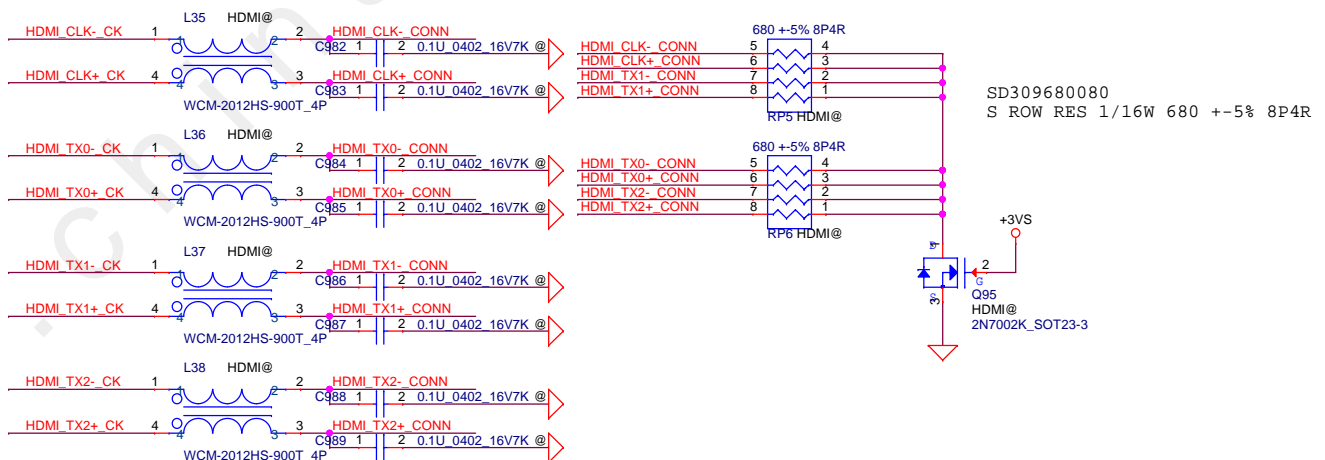
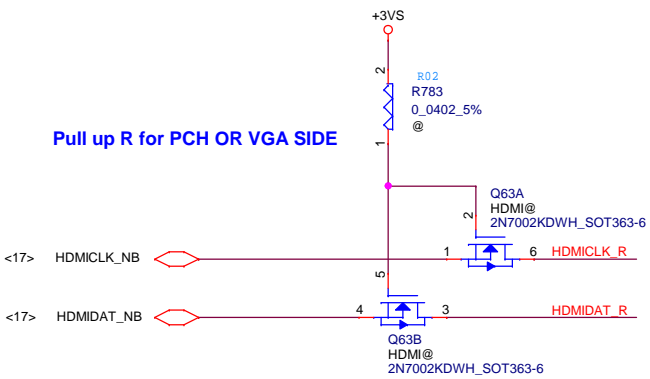


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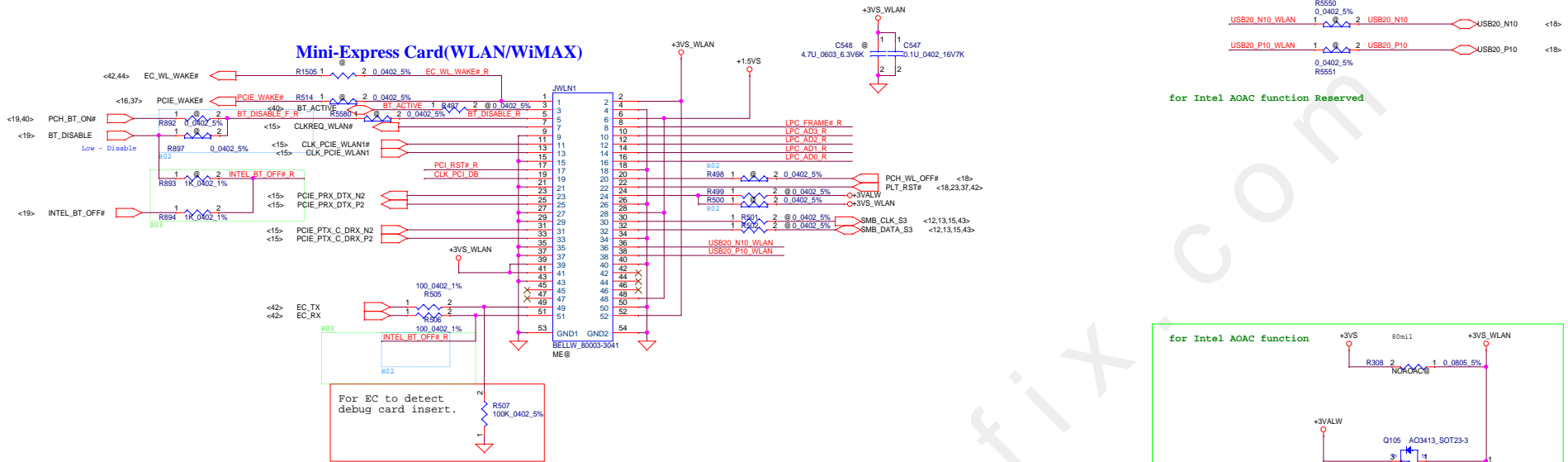


Pull up R for PCH OR VGA SIDE



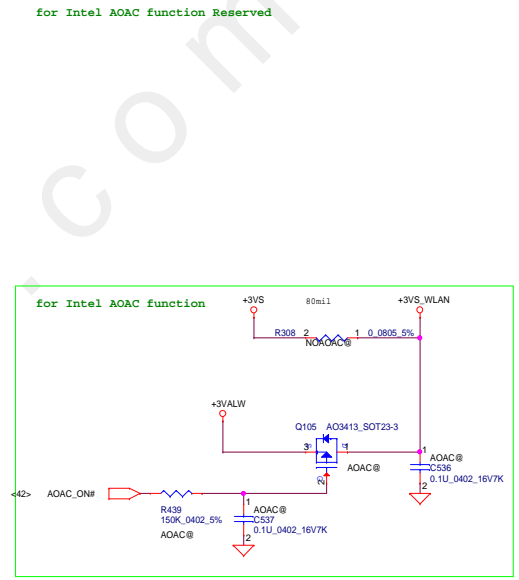
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				Document Number	Rev
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# Mini-Express Card for WLAN/WiMAX(Half)

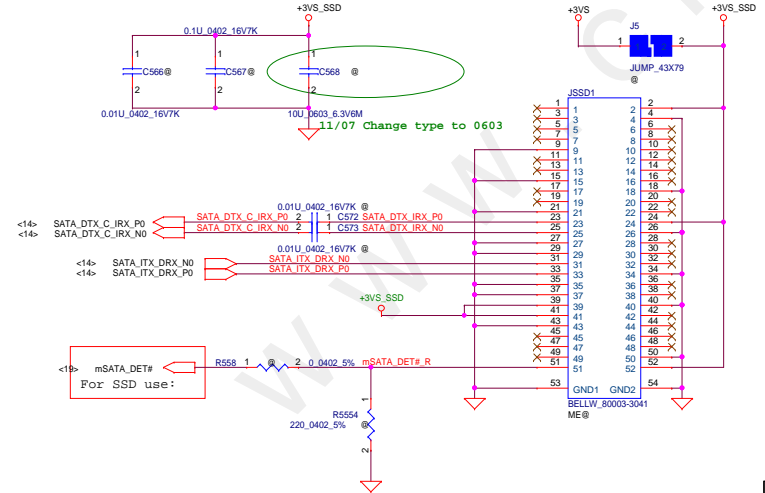


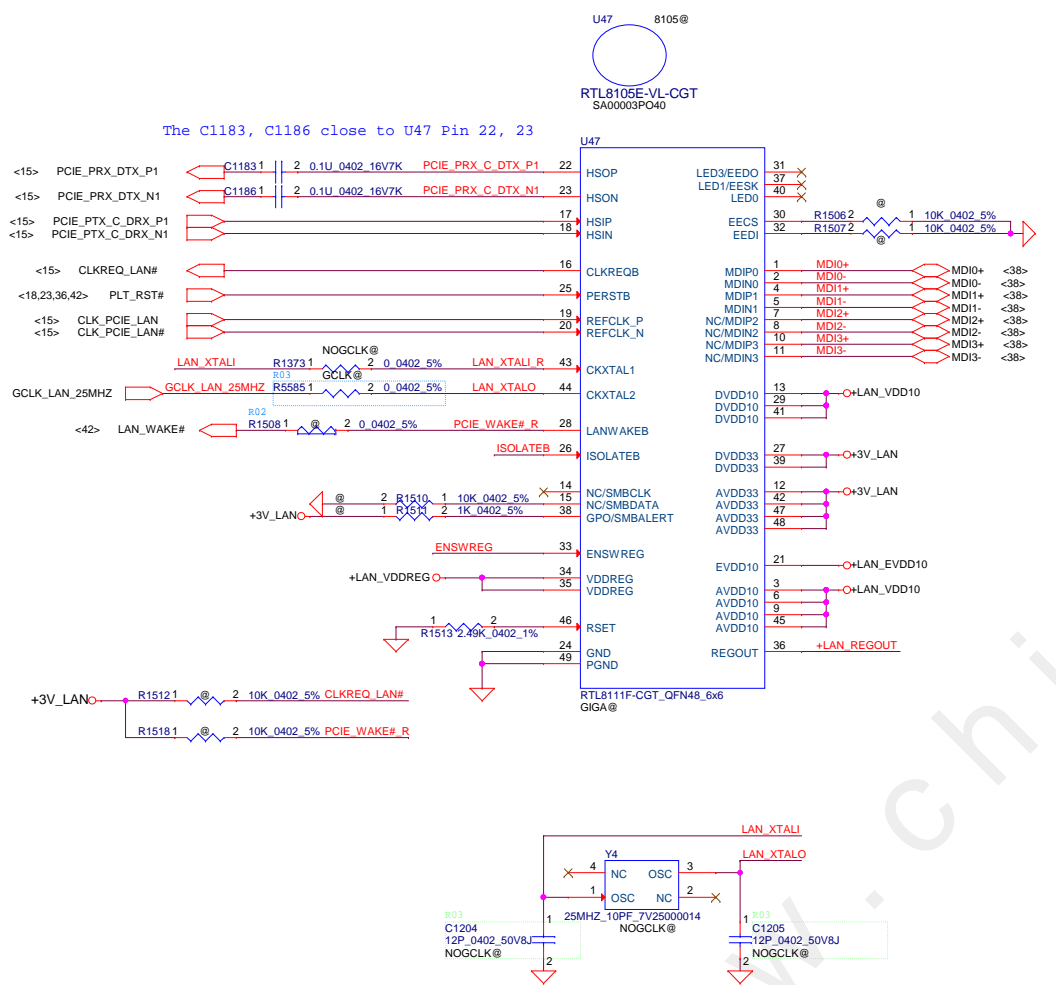
**Reserve for SW mini-pcie debug card.**  
Series resistors closed to KBC side.

LPC_FRAME# R	R508	1	@	2	0.0402_5%	LPC_FRAME#	<14,42>
LPC_AD3 R	R509	1	@	2	0.0402_5%	LPC_AD3	<14,42>
LPC_AD2 R	R510	1	@	2	0.0402_5%	LPC_AD2	<14,42>
LPC_AD1 R	R511	1	@	2	0.0402_5%	LPC_AD1	<14,42>
LPC_AD0 R	R512	1	@	2	0.0402_5%	LPC_AD0	<14,42>
PLT_RST#	R500	1	@	2	0.0402_5%	PLT_RST#	<18,23,37,42>
CLK_PCI_DB	R513	1	@	2	0.0402_5%	CLK_PCI_DB	<18>

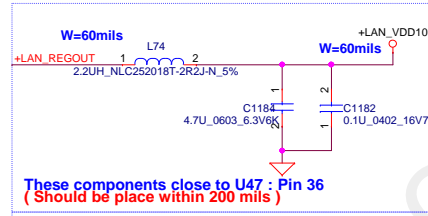
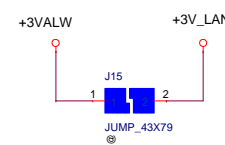


## Mini-Express Card(SSD) SSD Active:4.5W(1.5A)

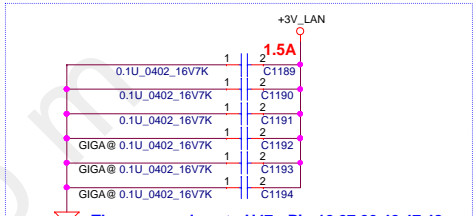




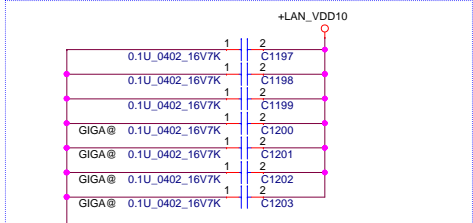
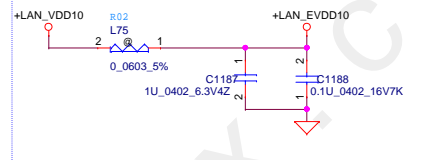
The C1183, C1186 close to U47 Pin 22, 23



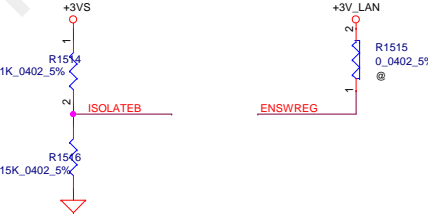
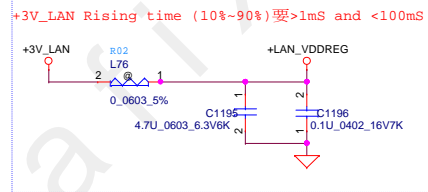
These components close to U47 : Pin 36 (Should be place within 200 mils)



These caps close to U47 : Pin 12,27,39,42,47,48



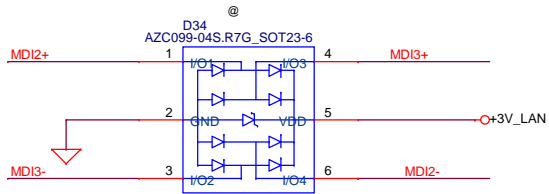
These caps close to U47 : Pin 3,6,9,13,29,41,45



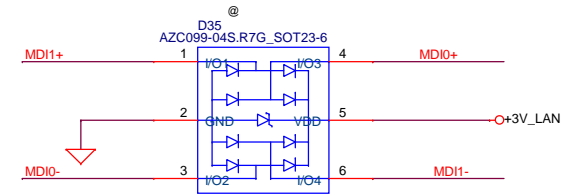
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Reserve gas tube for EMI go rural solution

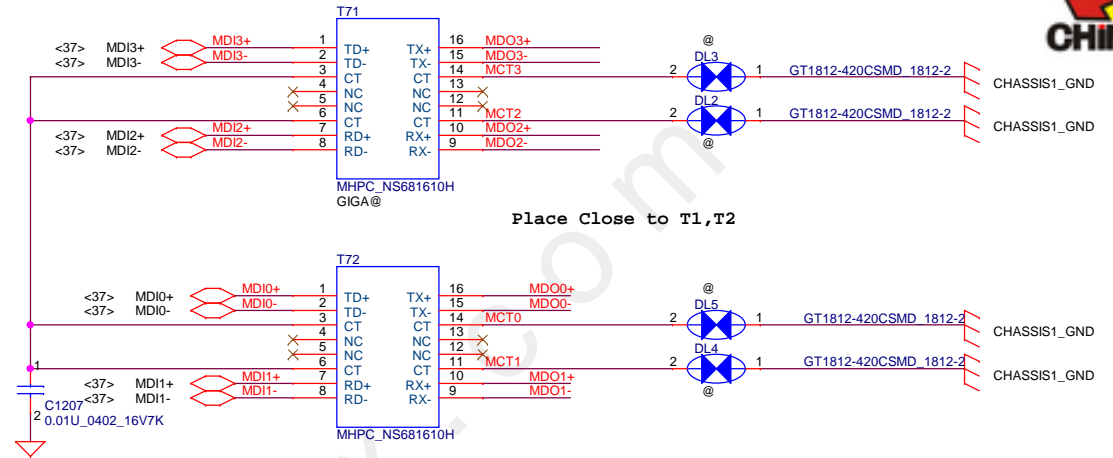


Place Close to T71

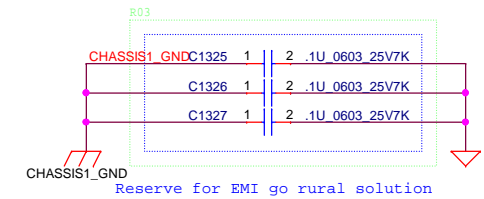
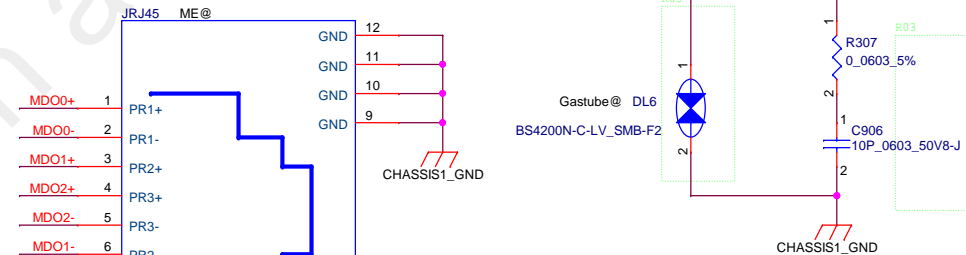
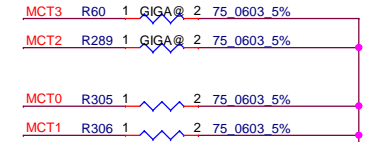


Place Close to T72

D34/D35  
1'S PN:SC300001G00  
2'S PN:SC300002E00



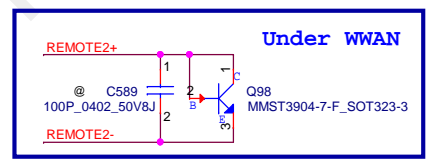
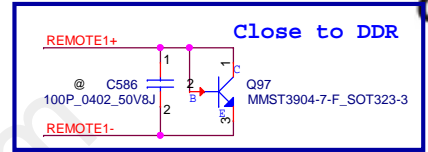
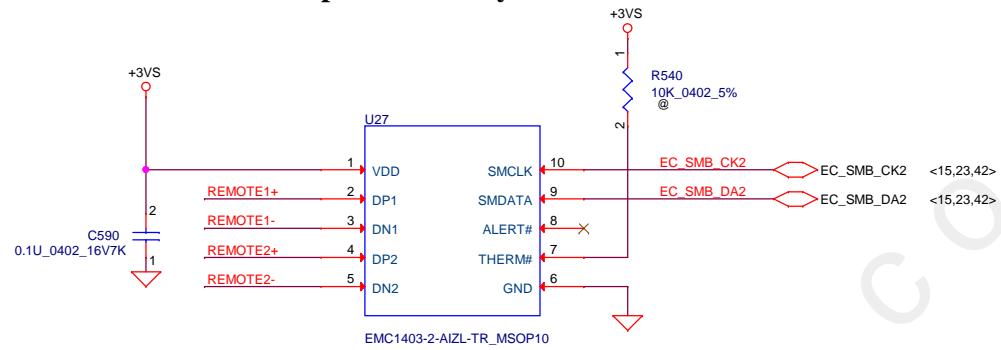
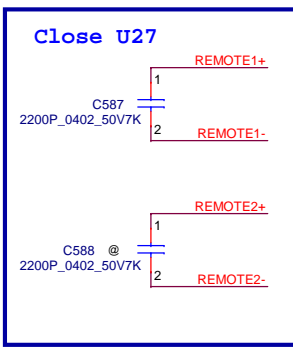
Place Close to T1,T2



Reserve for EMI go rural solution

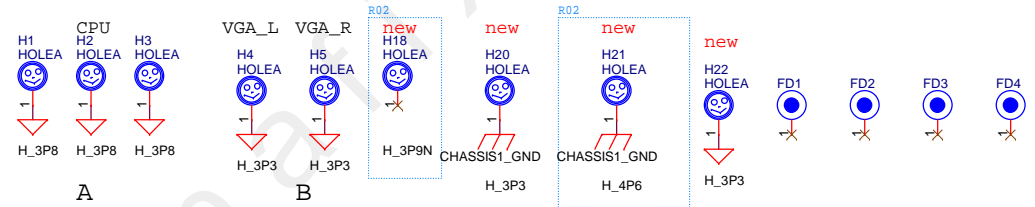
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Issued Date	2012/12/26	Deciphered Date	2012/07/11	Title LAN_Transformer		
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				Date:	Wednesday, January 09, 2013	Sheet 38 of 62

### SMSC thermal sensor placed near by VRAM

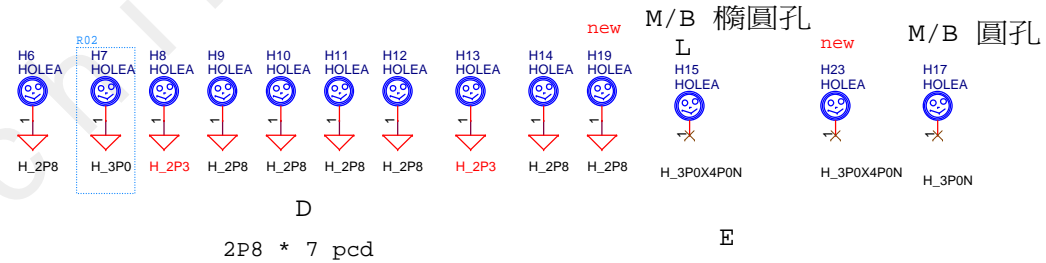
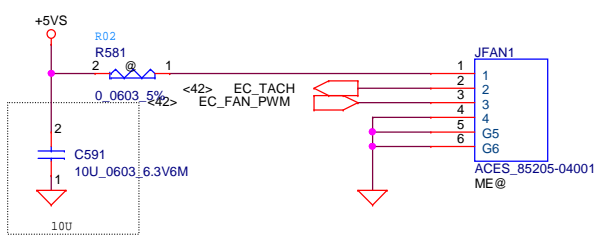


**REMOTE1,2+/-:**  
Trace width/space:10/10 mil  
Trace length:<8"

Address 1001\_101xb



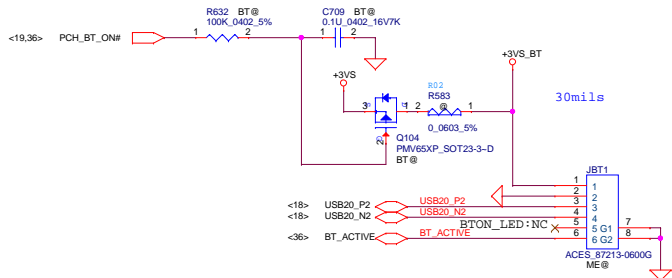
### FAN1 Conn



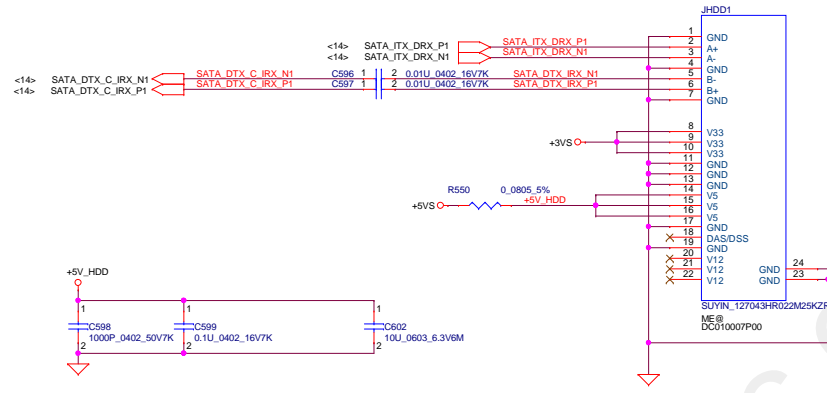
Security Classification	Compal Secret Data			<b>Compal Electronics, Ltd.</b>	
Issued Date	2012/12/26	Deciphered Date	2012/07/11	Title	<b>Fintek-Thermal IC/FAN/screw</b>
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				Date	Wednesday, January 09, 2013



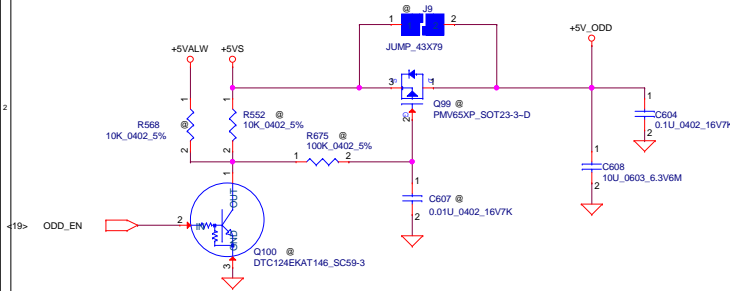
### BT MODULE CONN



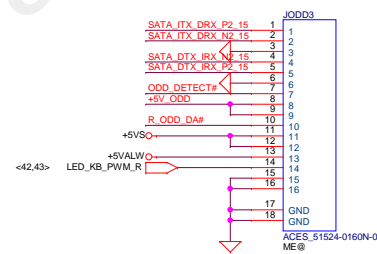
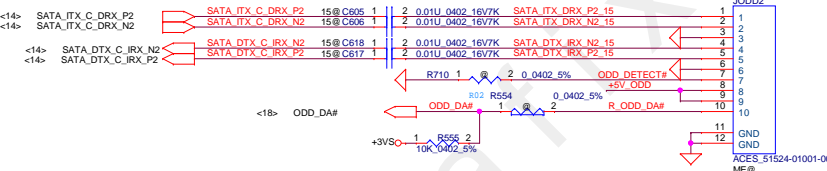
### SATA HDD Conn.



### ODD Power Control

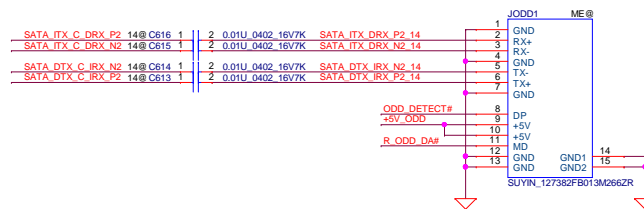


### FOR 15" SATA ODD FFC Conn.



Co-lay

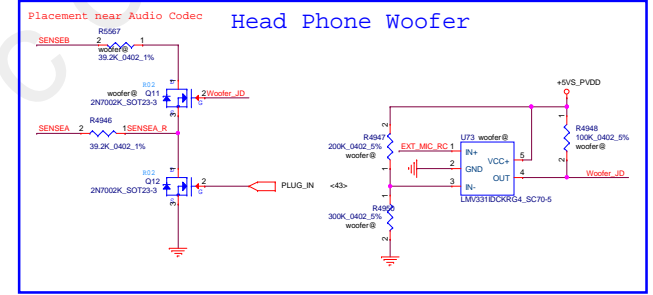
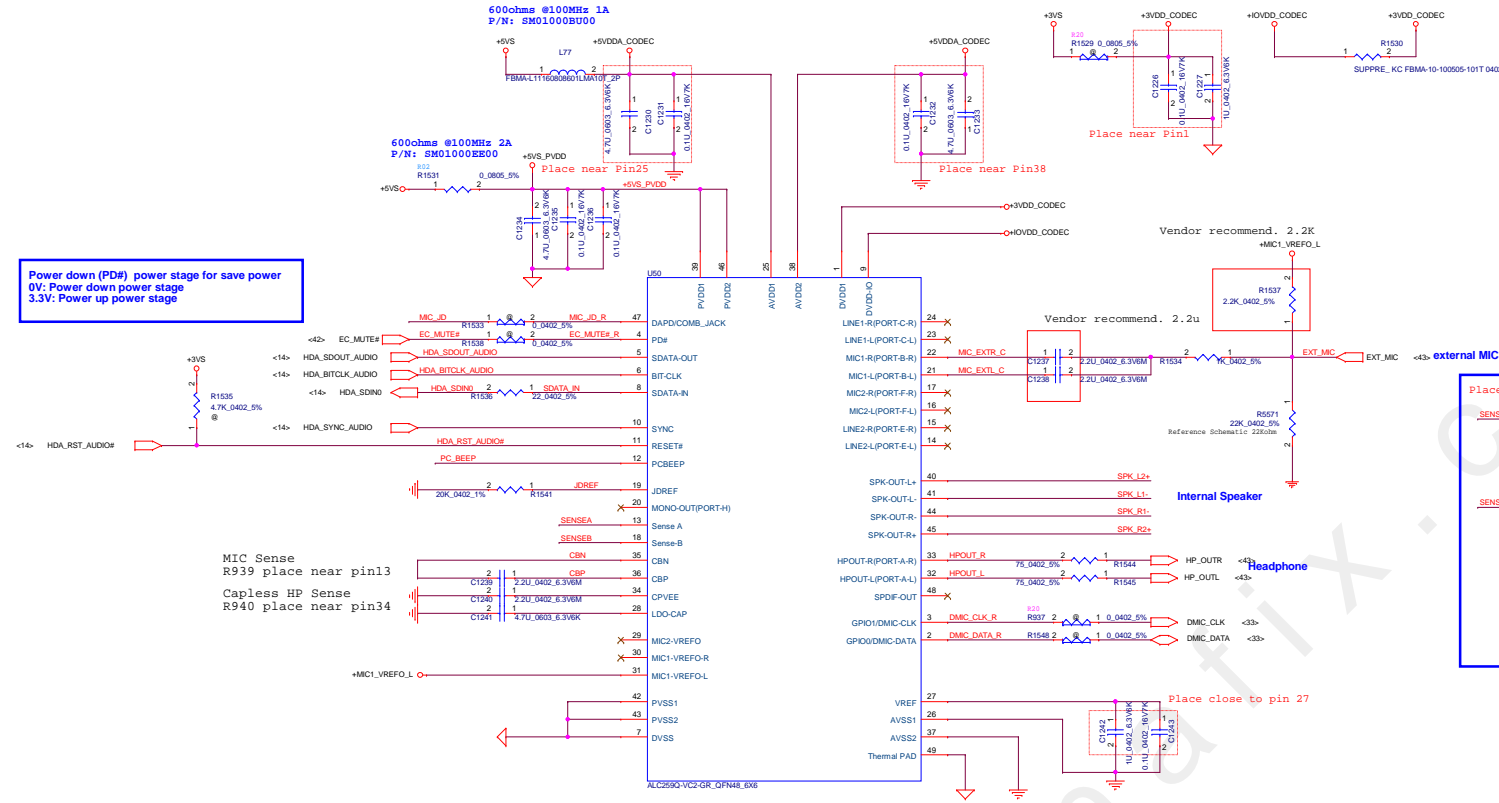
### FOR 14" SATA ODD Conn.



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Date:	Wednesday, January 03, 2013	Sheet	40	of 62



Power down (PD#) power stage for save power  
 DV: Power down power stage  
 3.3V: Power up power stage

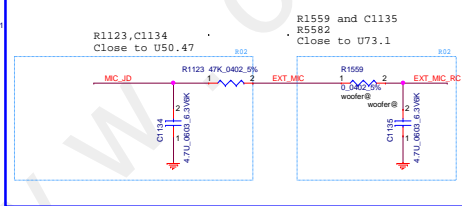


Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1 (Pin21/22)	External	Mic in

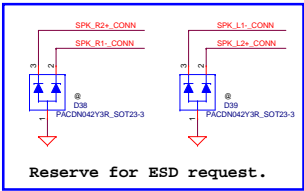
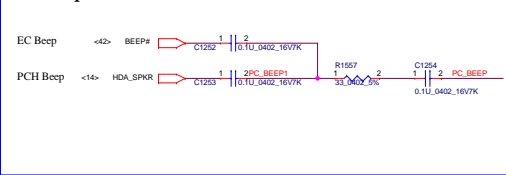
wide 25MIL

SPK L+L-R+R- trace width  
 Speaker 4 ohm =>40 mils  
 Speaker 8 ohm =>20 mils

Combo Jack detect (normal open)



PC BEEP



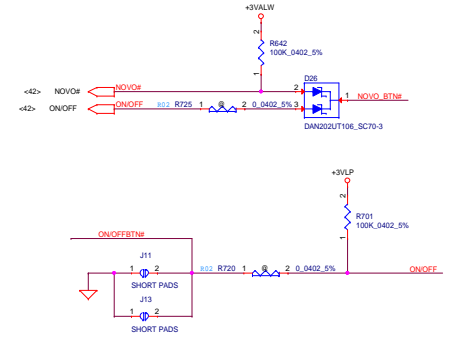
Reserve for ESD request.

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Date: Wednesday, January 09, 2013			Sheet	41 of 62

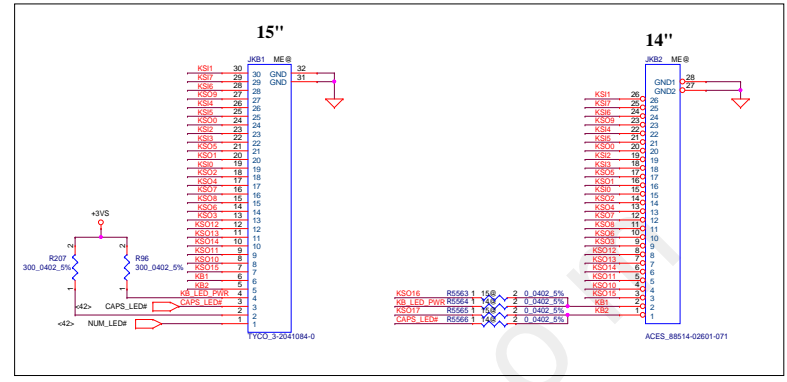




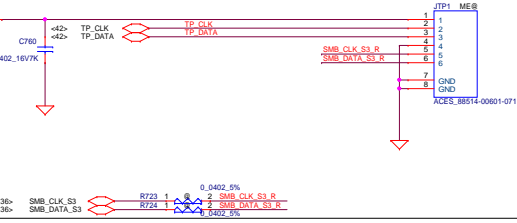
### ON/OFF switch



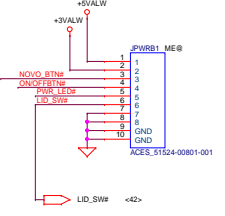
### K/B Connector



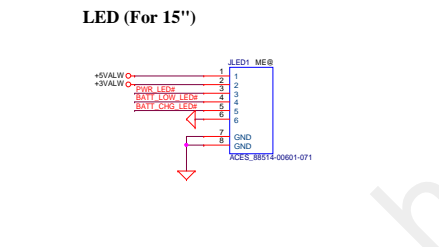
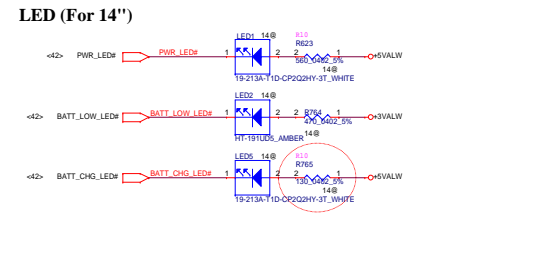
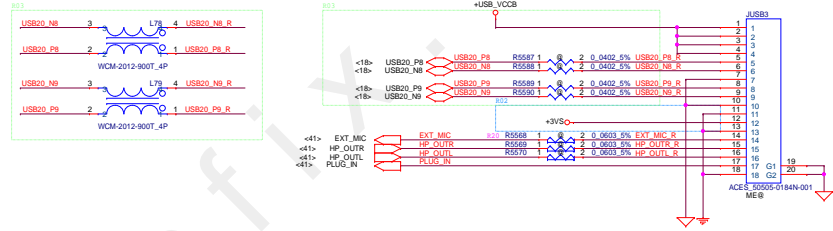
### TP/B Connector



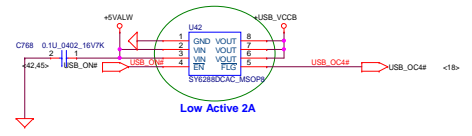
### PWR/B Connector



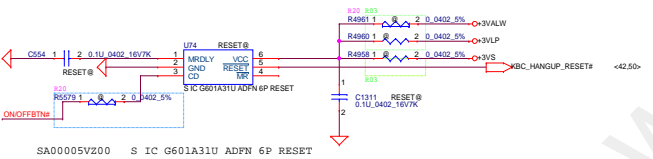
### USB I/O Connector



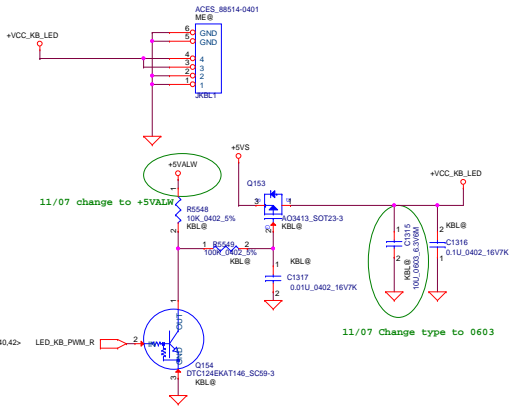
### Right Side USB2.0 Port X 2 (USB/B)



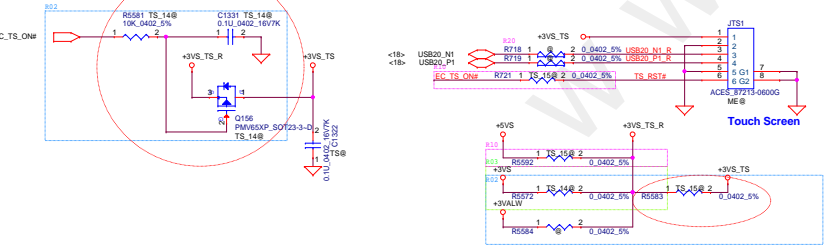
### EC RESEST function



### KB Lighting CONN.4pin

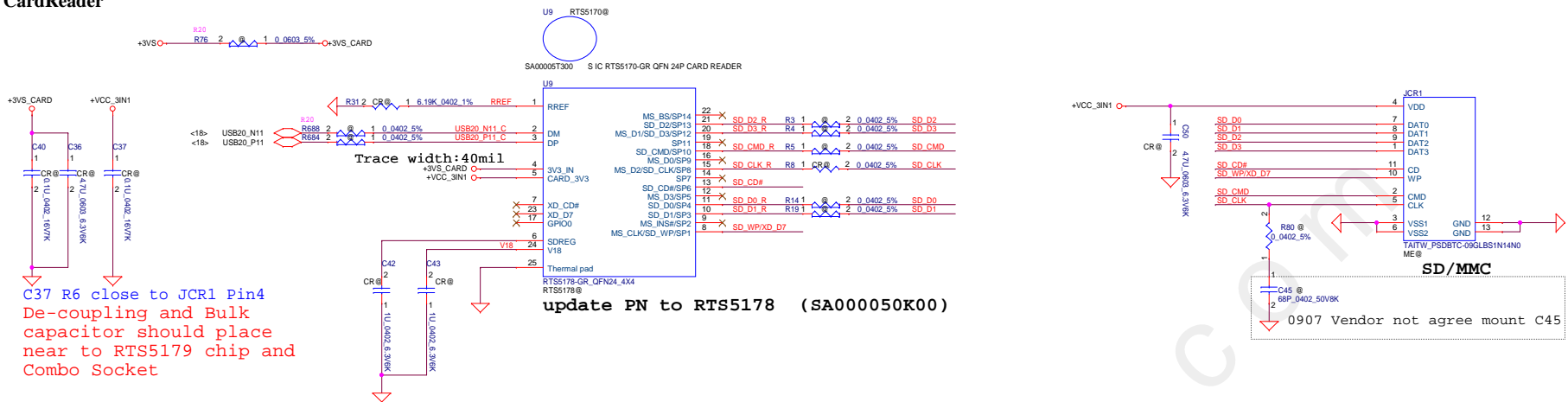


### Touch Screen



Security Classification	Compal Secret Data		Title	ROM/KBD/PWR/CR/LED/TP Conn.
Issued Date	2012/2/26	Deciphered Date	2012/07/11	Doc. Number
				LA-9603P
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RTS5178 CardReader

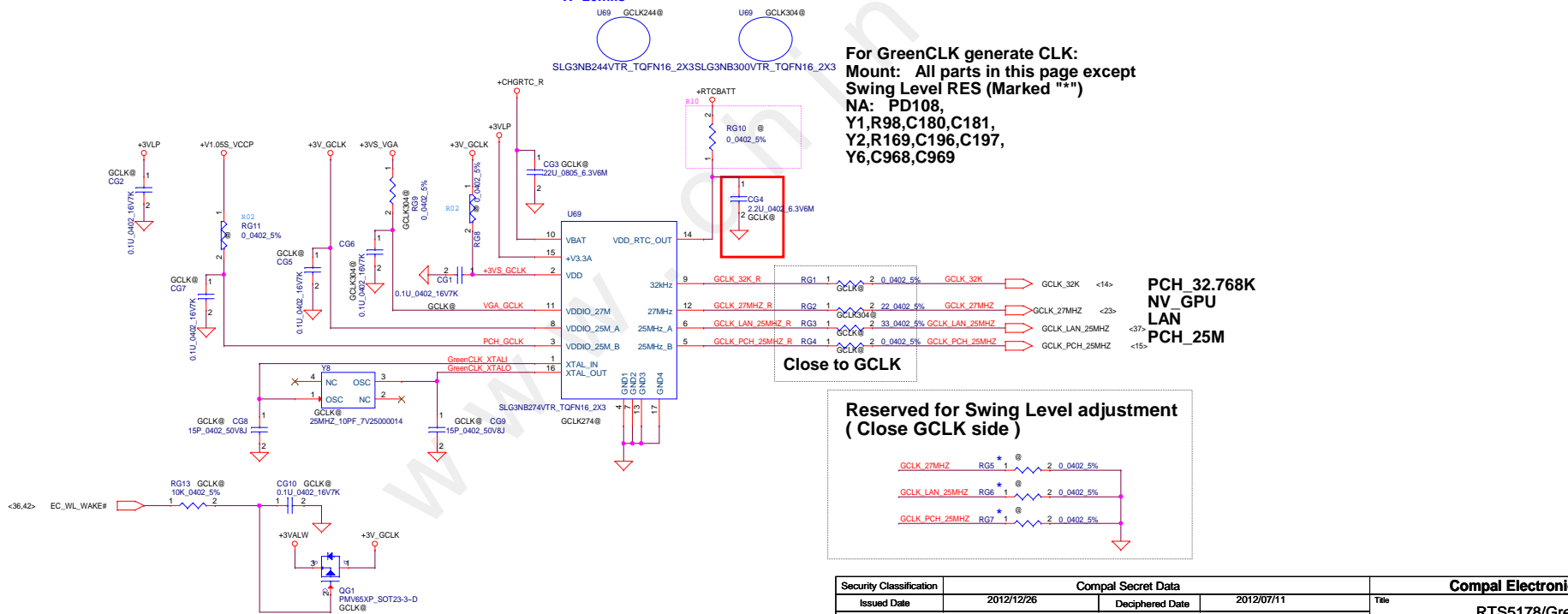


C37 R6 close to JCR1 Pin4  
De-coupling and Bulk capacitor should place near to RTS5179 chip and Combo Socket

Green Clock

Every power trace need: W=20mils

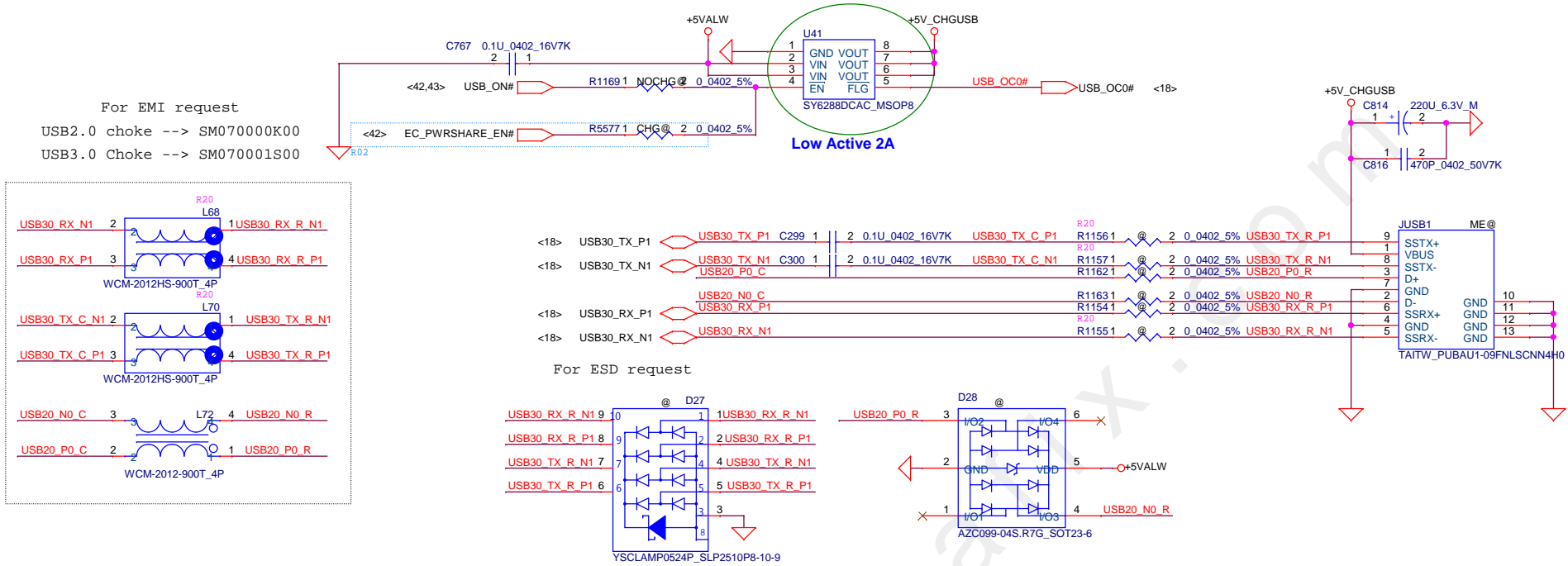
For GreenCLK generate CLK:  
Mount: All parts in this page except Swing Level RES (Marked "\*\*")  
NA: PD108, Y1,R98,C180,C181, Y2,R169,C196,C197, Y6,C968,C969



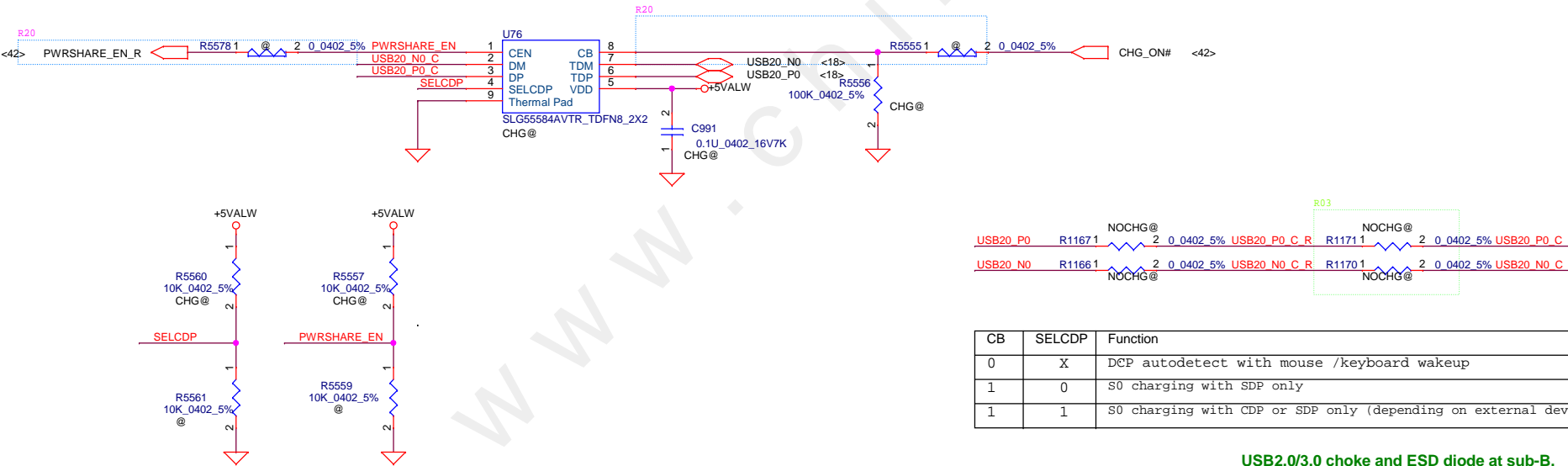
PCH\_32.768K  
NV\_GPU  
LAN  
PCH\_25M

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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Size	C	Document Number	LA-9603P	Rev 1.0
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## LEFT SIDE USB3.0 PORT X1



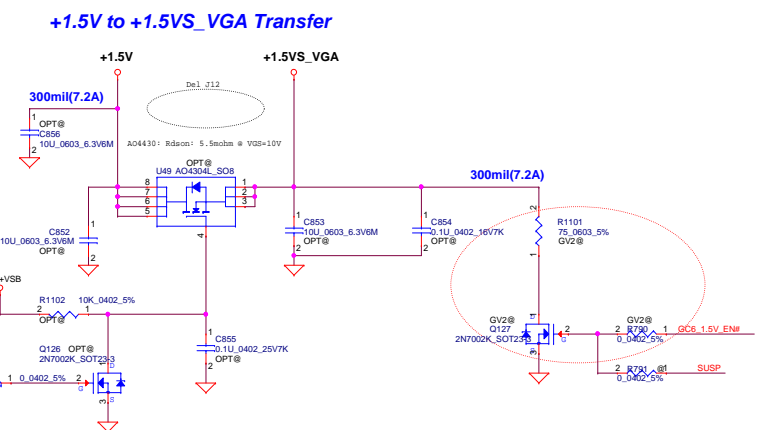
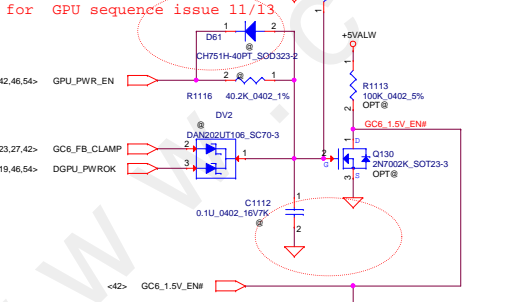
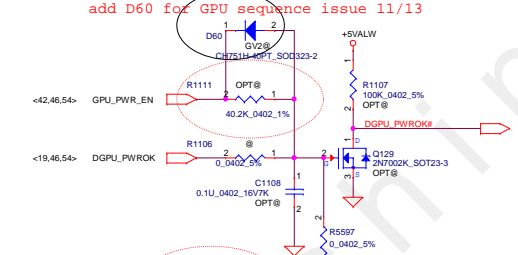
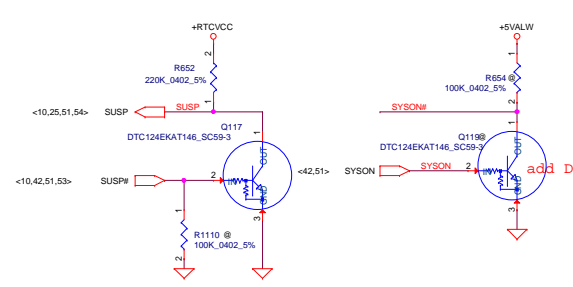
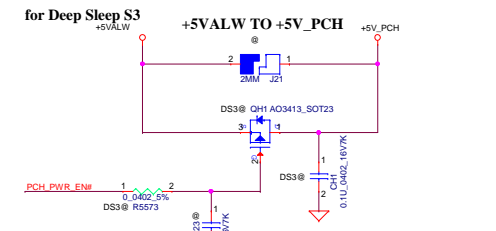
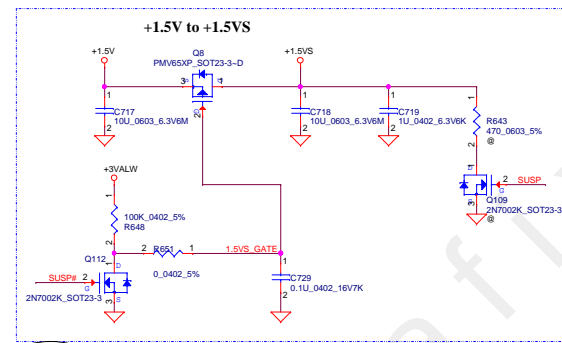
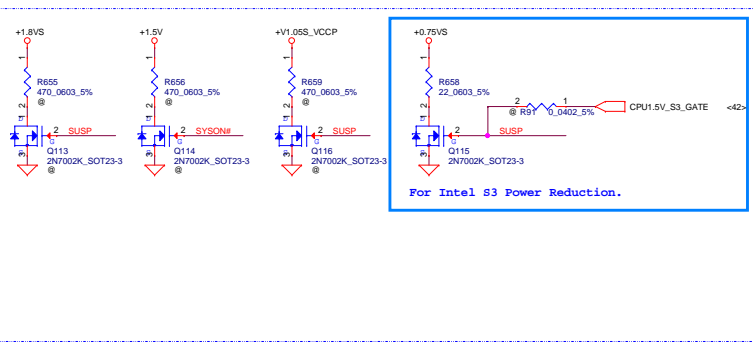
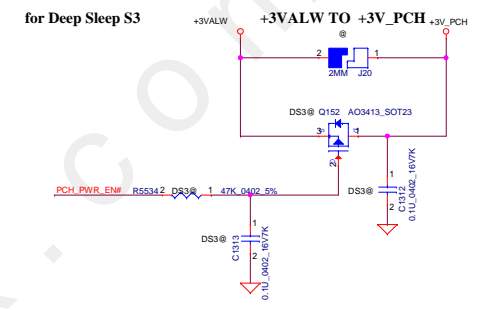
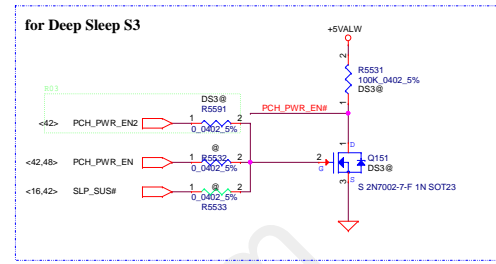
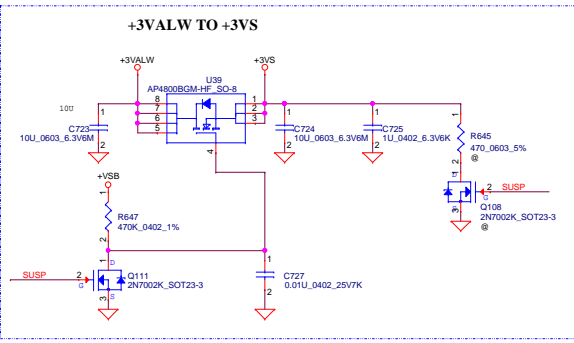
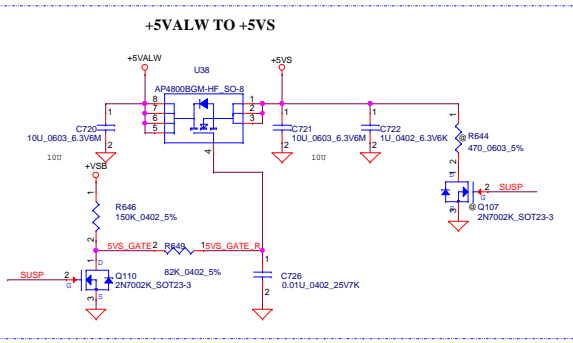
## Left Side Charger USB3.0 Port



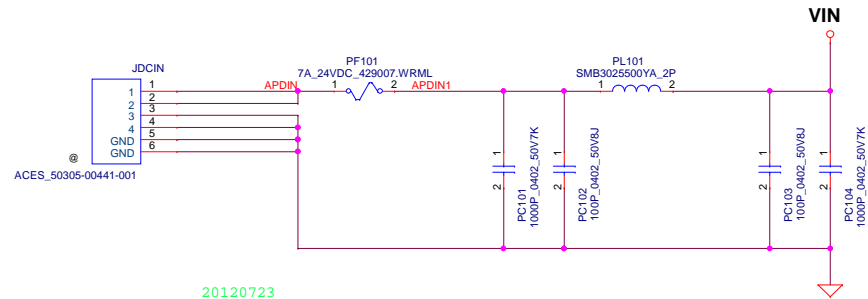
CB	SELCDP	Function
0	X	DCP autodetect with mouse /keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device )

USB2.0/3.0 choke and ESD diode at sub-B.

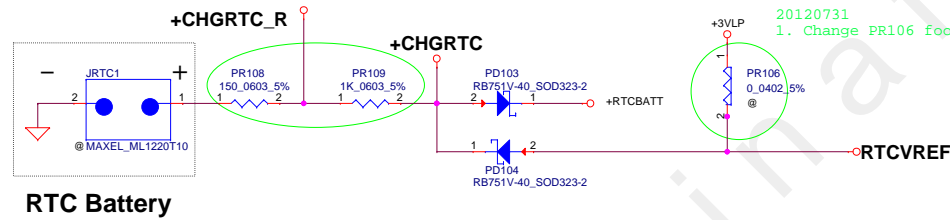
Security Classification		Compal Secret Data		Title	
Issued Date	2012/12/26	Deciphered Date	2012/07/11	USB3.0/Left USB Ports	
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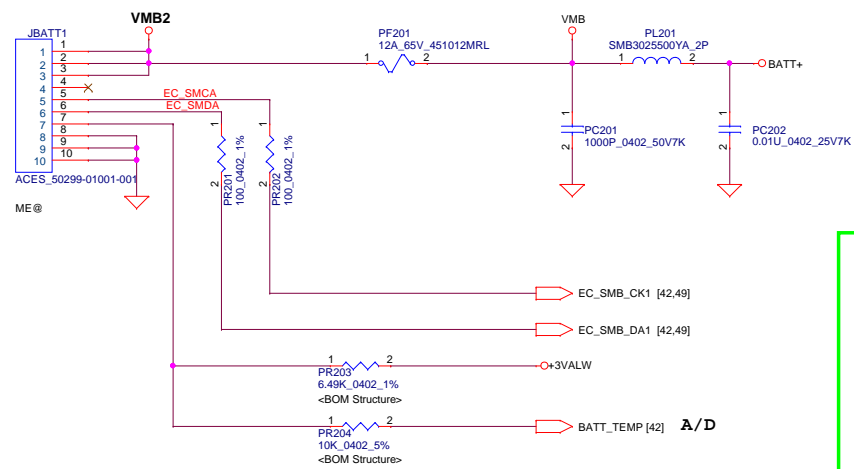
20120723  
 For all sku  
 1. Change PR108 to 150\_0603\_5% SD013150080 from 560\_0603\_5% SD013560080  
 Change PR109 to 1K\_0603\_5% SD013100180 from 560\_0603\_5% SD013560080



20120731  
 1. Change PR106 footprint to R0402\_0ohm-NEW

20120731  
 1. Add PR110 SD013000080 0\_0603\_5%  
 Add PR111 SD013150080 150\_0603\_5%

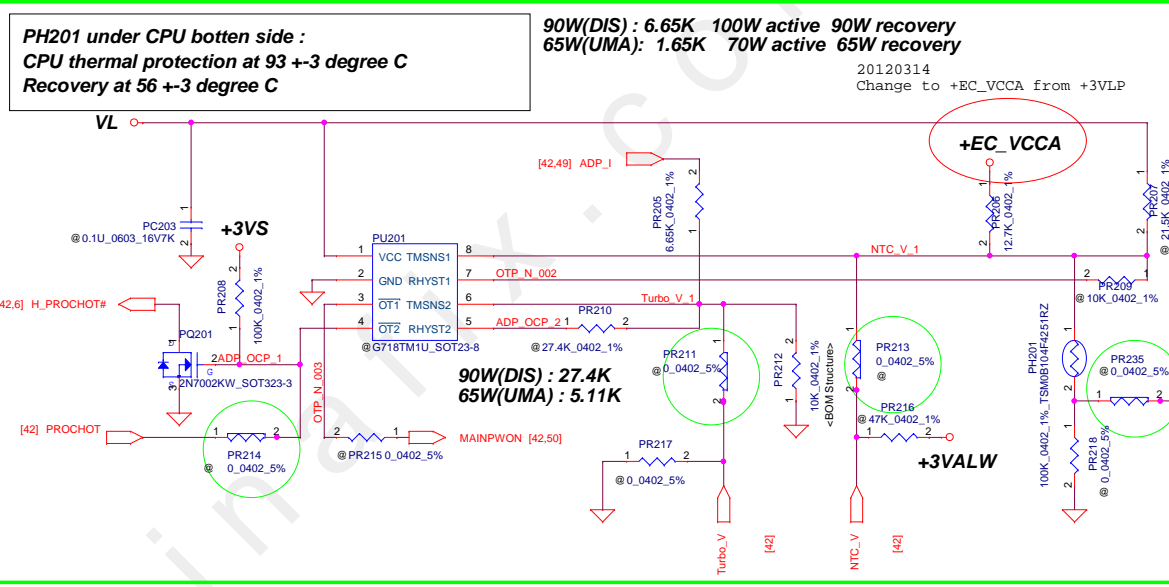
Security Classification	Compal Secret Data			Title	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	Compal Electronics, Inc.	
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				Document Number	0.1
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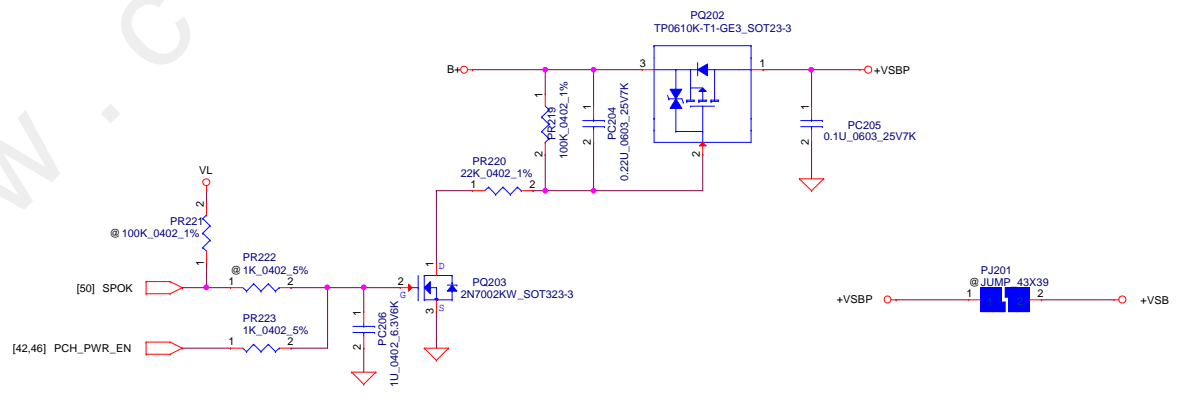
ADP\_I need to write Charge Options Register (0x12H)=> bit6=1

0: IOUT is the 20x current amplifier output <default @ POR>

1: IOUT is the 40x current amplifier output



20120731  
1. Change PR214, PR211, PR213 and PR235 footprint to R0402\_0ohm-NEW

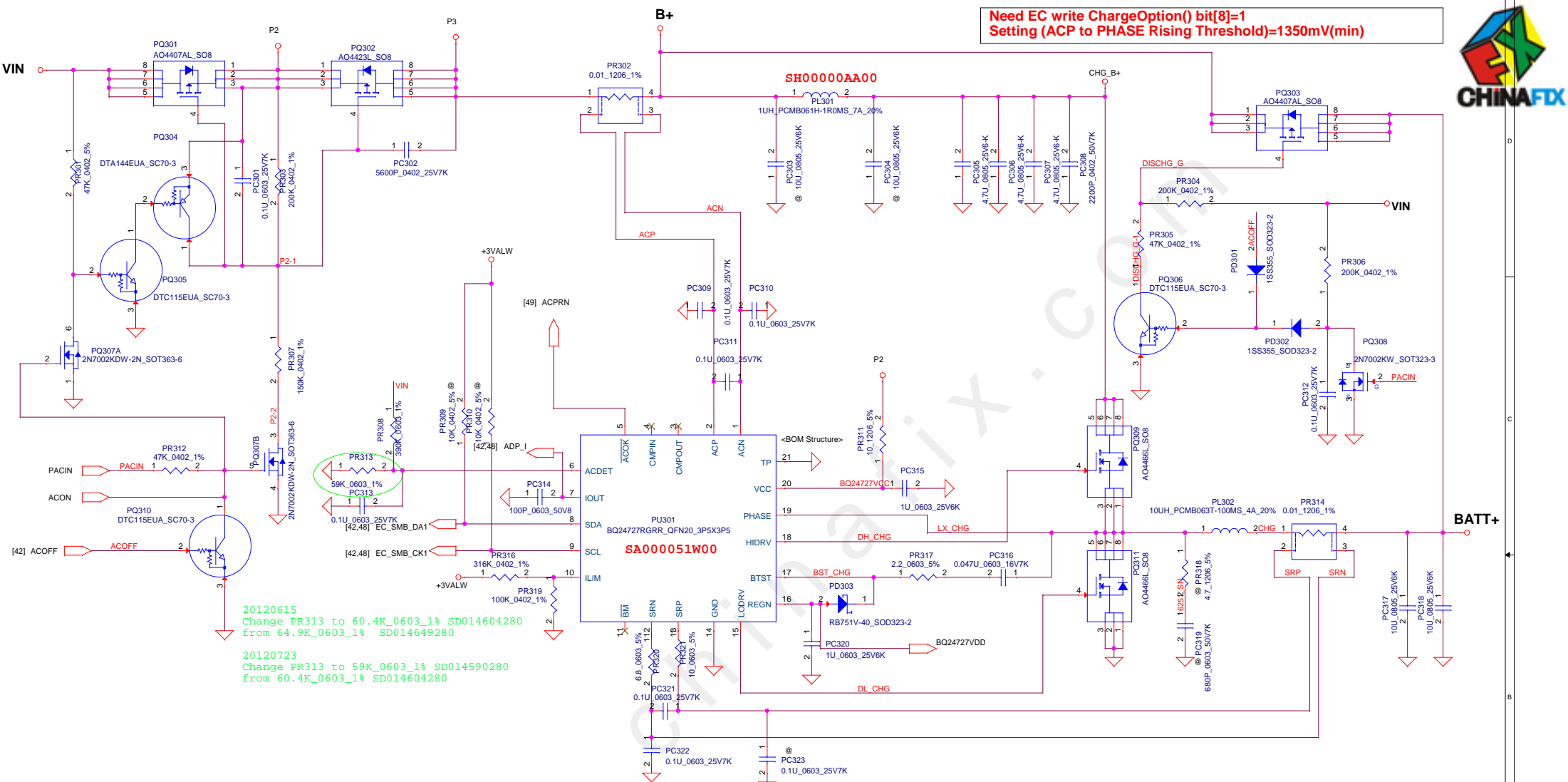


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				Zx90
				Rev
				0.1
				Date: Wednesday, January 09, 2013
				Sheet 48 of 62



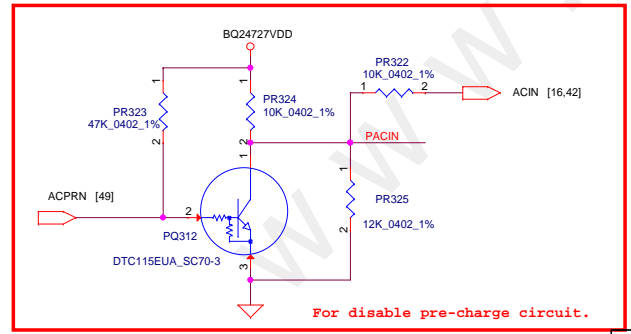


Need EC write ChargeOption() bit[8]=1  
Setting (ACP to PHASE Rising Threshold)=1350mV(min)



20120615  
Change PR313 to 60.4K\_0603\_1% SD014604280  
from 64.9K\_0603\_1% SD014649280

20120723  
Change PR313 to 59K\_0603\_1% SD014590280  
from 60.4K\_0603\_1% SD014604280



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				<b>CHARGER</b>	
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				Date: Wednesday, January 09, 2013	Sheet 49 of 62



20120321  
Change netname to CPU\_B+ from B+

**CPU\_B+**

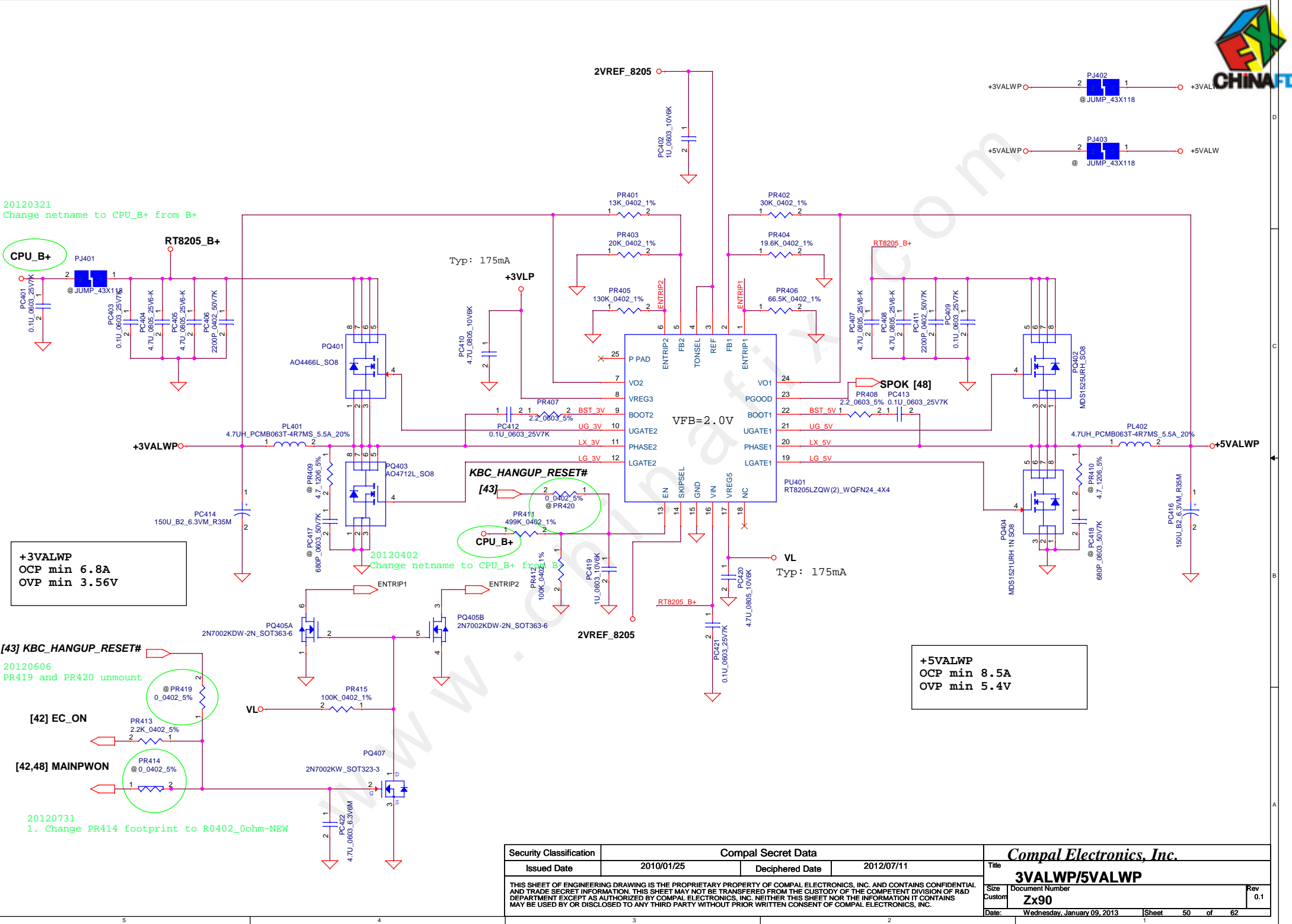
**+3VALWP**  
OCP min 6.8A  
OVP min 3.56V

**[43] KBC\_HANGUP\_RESET#**  
20120606  
PR419 and PR420 unmount

**[42] EC\_ON**

**[42,48] MAINPWON**

20120731  
1. Change PR414 footprint to R0402\_0ohm-NEW

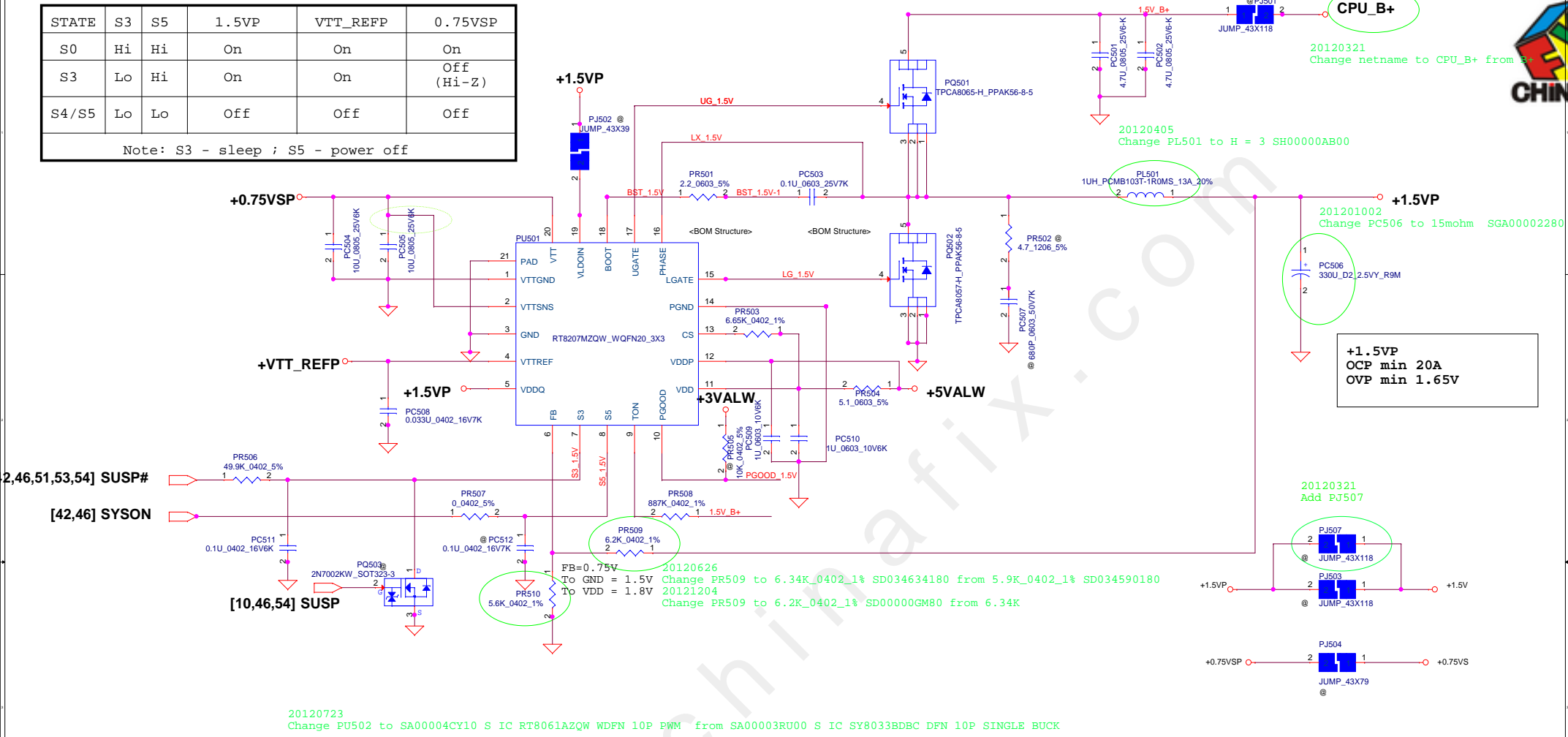


Security Classification		Compal Secret Data		Title	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	3VALWP/5VALWP	
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Wednesday, January 09, 2013				50	62



STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



[2,46,51,53,54] SUSP#

[42,46] SYSON

[10,46,54] SUSP

[10,25,42,46,51,53,54] SUSP#

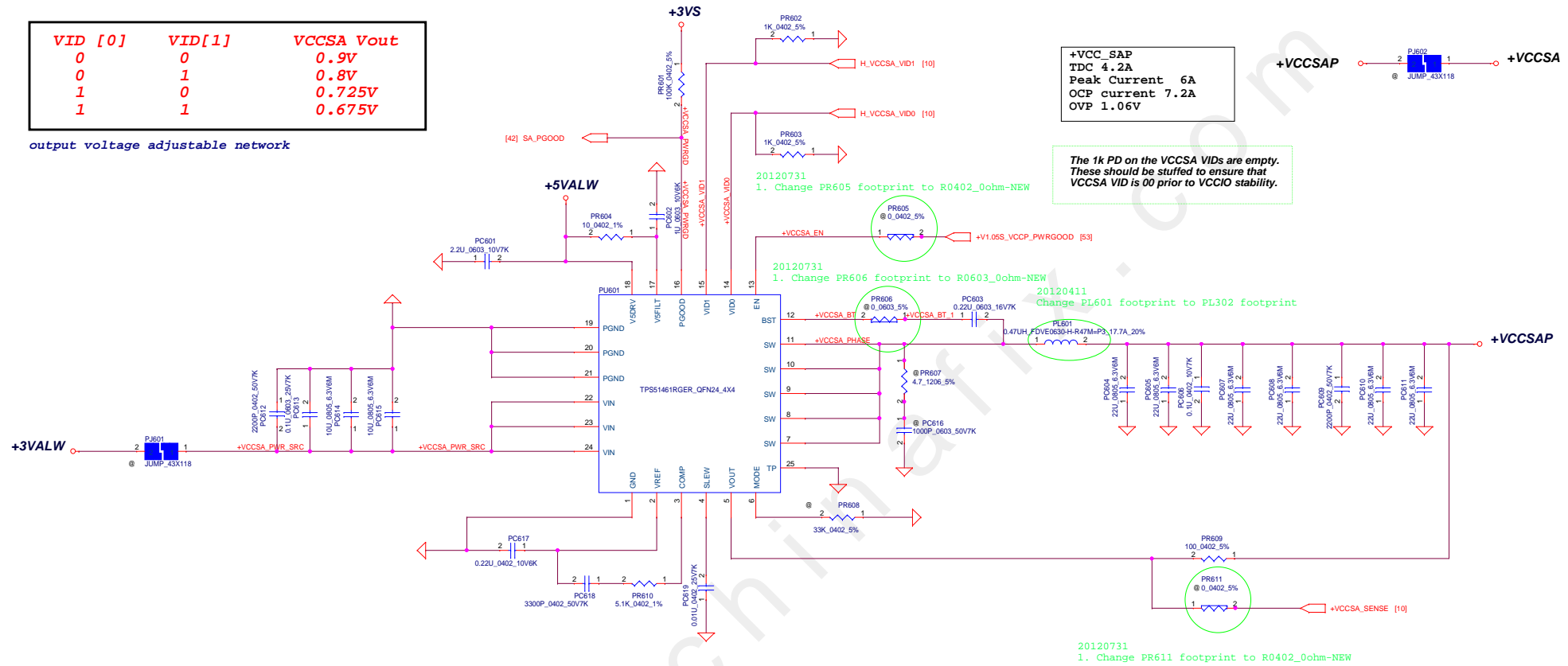
+1.8VP  
current limit min 4A

1.8VSP max current=4A

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	+1.5VP/+1.8VSP
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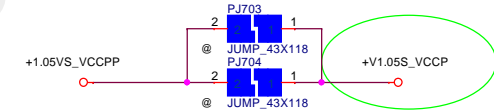
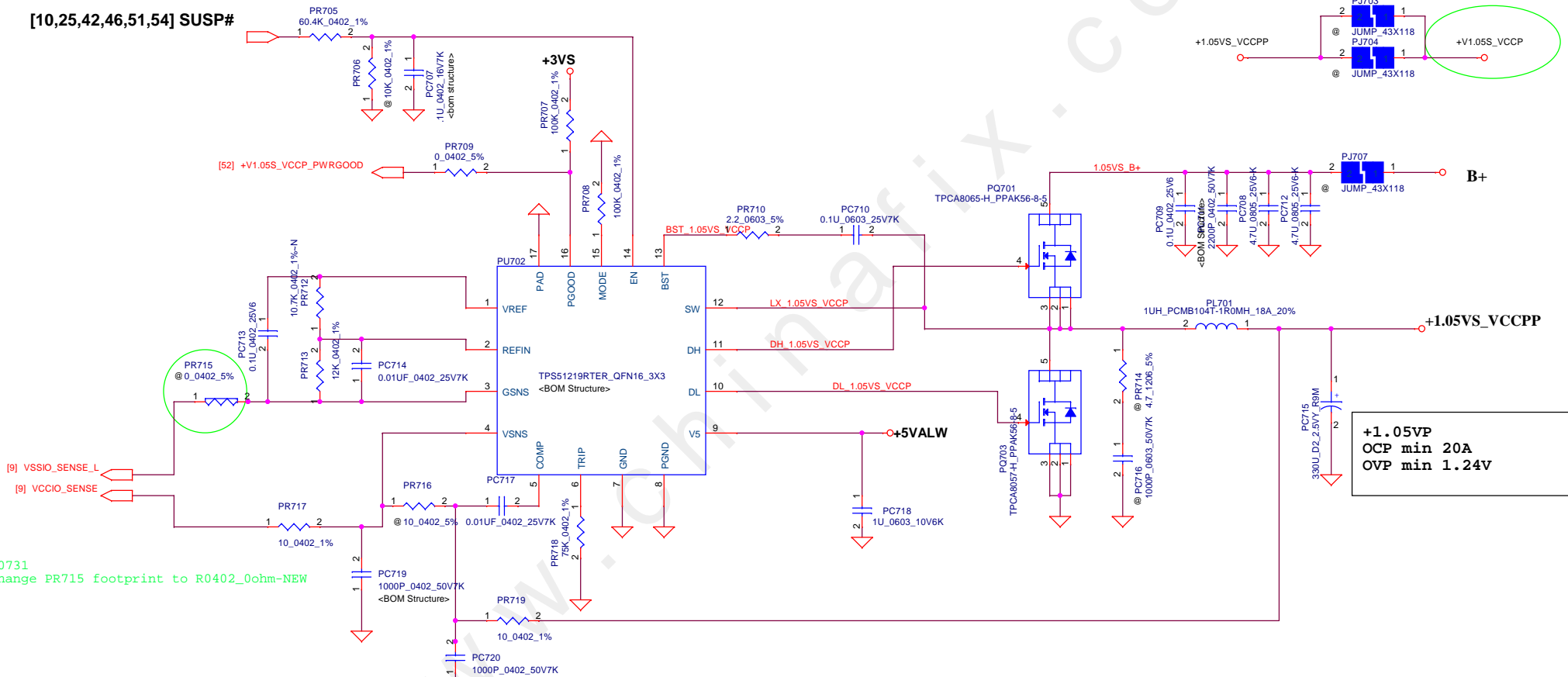
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



[10,25,42,46,51,54] SUSP#

20120330  
Change net name to +V1.05S\_VCCP from +1.05S\_VCCP



+1.05VP  
OCP min 20A  
OVP min 1.24V

20120731  
1. Change PR715 footprint to R0402\_0ohm-NEW

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Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	+1.05VS VCCP
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- 20121015  
 1.Change PR816 from SD028100380 S RES 1/16W 100K +-5% 0402 to SD028100180 S RES 1/16W 1K +-5% 0402  
 2.Change PQ803 from NA to SB000009Q80 S TR 2N7002KW 1N SOT323-3  
 3.Change PR813 from NA to SD000001R80 S RES 1/10W 22 +-5% 0603  
 4.Change PR815 from NA to SD028000080 S RES 1/16W 0 +-5% 0402

- 20120405  
 Change PQ802 and PJ802 netname to +V1.05S\_VCCP from +1.05VS

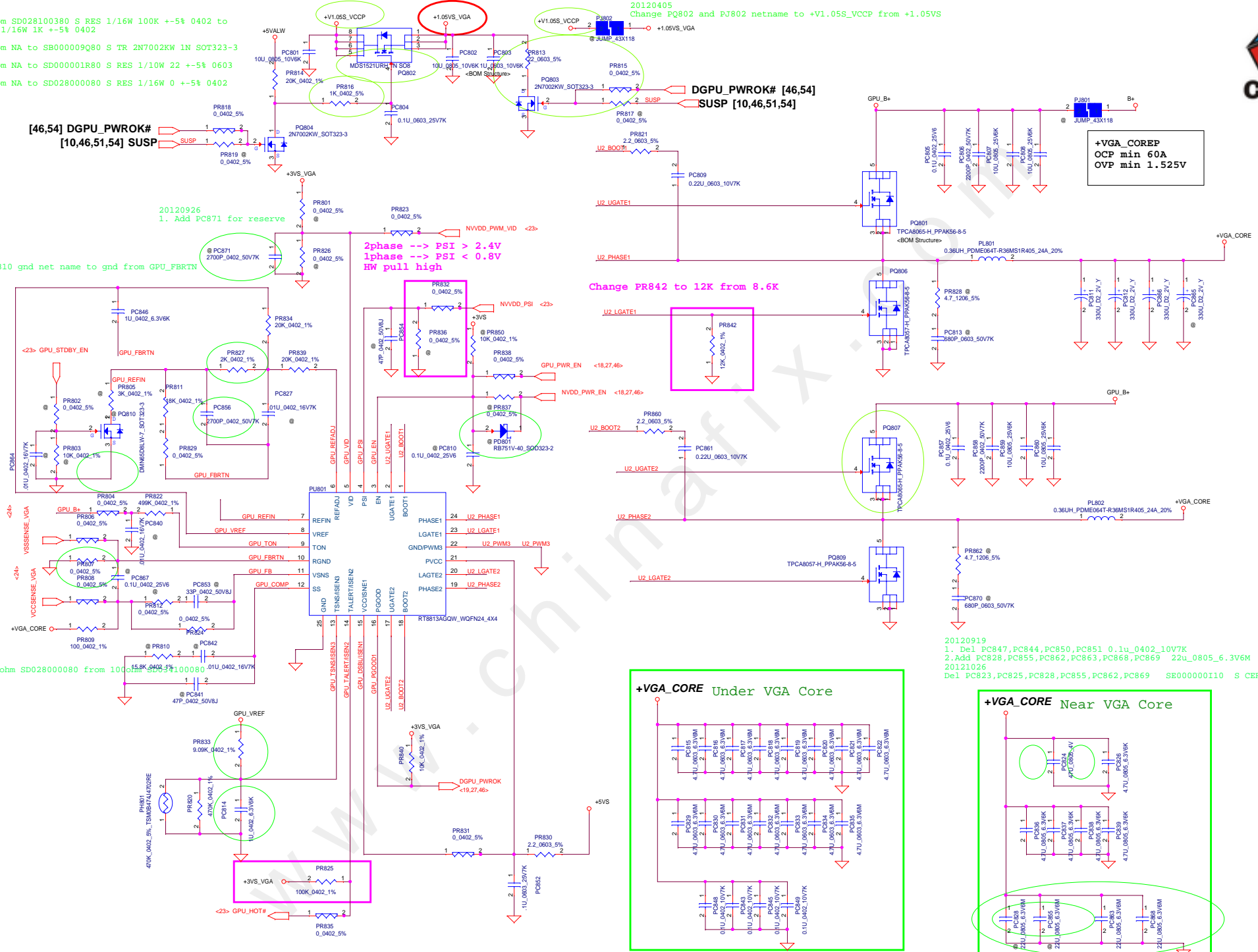
[46,54] DGPU\_PWROK#  
 [10,46,51,54] SUSP

20120926  
 1. Add PC871 for reserve

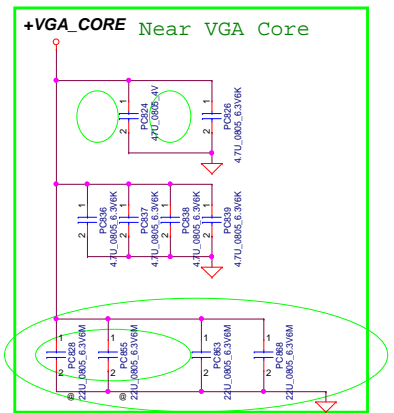
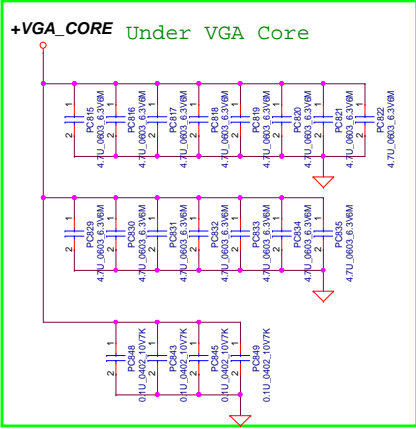
20120919  
 1. Change PQ810 gnd net name to gnd from GPU\_FBR1N

2phase ---> PSI > 2.4V  
 1phase ---> PSI < 0.8V  
 HW pull high

Change PR842 to 12K from 8.6K



+VGA\_COREP  
 OCP min 60A  
 OVP min 1.525V



- 20120919  
 1. Del PC847, PC844, PC850, PC851 0.1u\_0402\_10V7K  
 2. Add PC828, PC855, PC862, PC863, PC866, PC869 22u\_0805\_6.3V6M  
 20121026  
 Del PC823, PC825, PC828, PC855, PC862, PC869 SE000001I10 S CER CAP 22UF 6.3V M X5

- 20121023  
 1.Change PR807 to 0ohm SD028000080 from 100ohm SD031000080 01U\_0402\_16V7K

Security Classification		Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2012/07/11	VGA COREP	
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				LA-9601P	Rev 0.1
				Date: Wednesday, January 09, 2013	Sheet 54 of 62

20120514  
 Change PH901, PH904 to SL200000L00 220K\_0402\_5%\_TSM0B224J4702RE  
 from SL2000000500 220K\_0402\_5%\_BRTJ0B224J

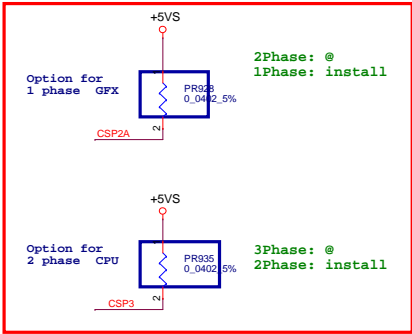
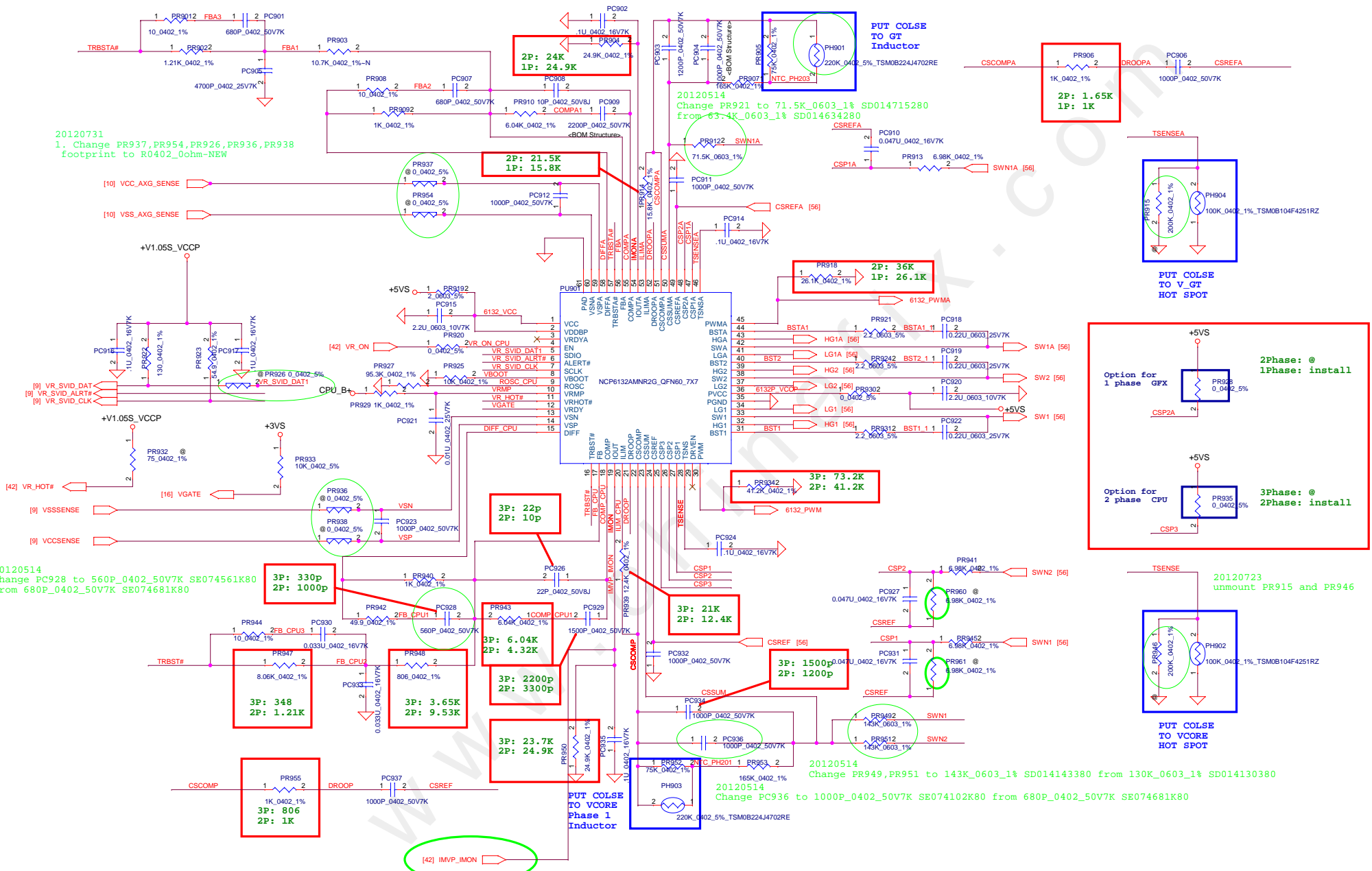
PR915, PR946=200K(setting 113 degreeC)  
 PR915, PR946=8.25K(setting 93 degreeC)

20120731  
 1. Change PR937, PR954, PR926, PR936, PR938  
 footprint to R0402\_0ohm-NEW

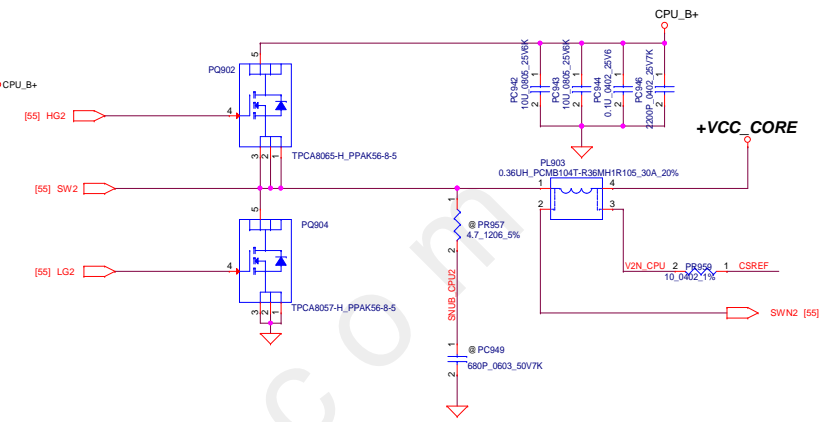
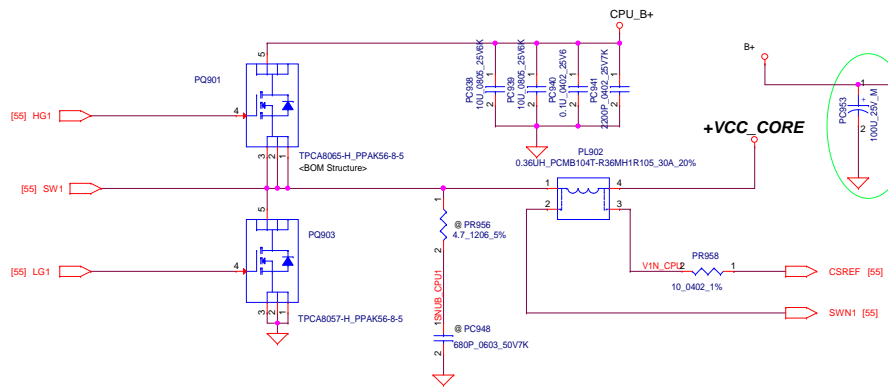
20120514  
 Change PR921 to 71.5K\_0603\_1%\_SD014715280  
 from 63.4K\_0603\_1%\_SD014634280

20120514  
 Change PR949, PR951 to 143K\_0603\_1%\_SD014143380 from 130K\_0603\_1%\_SD014130380

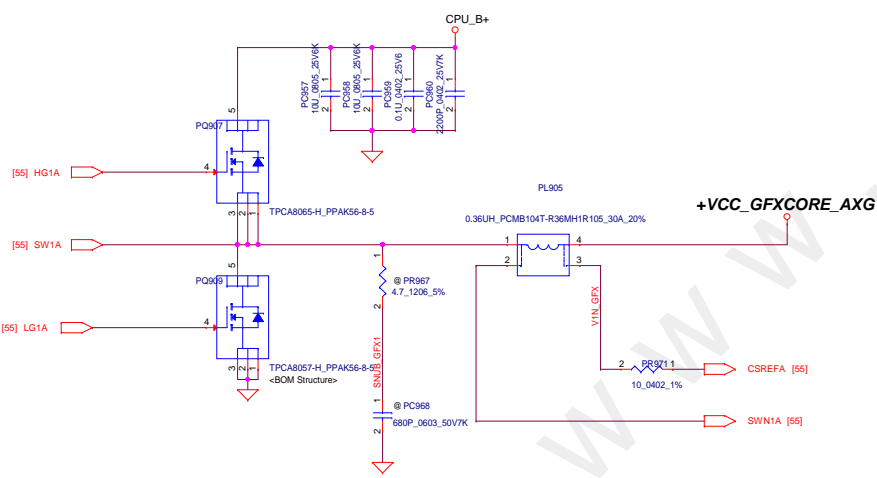
20120514  
 Change PC936 to 1000P\_0402\_50V7K SE074102K80 from 680P\_0402\_50V7K SE074681K80



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Document Number	C38-G series Chief River Schematic			Rev	0.1
Date	Wednesday, January 06, 2013	Sheet	55	of	62



DC 35W CPU  
 VID1=1.05V  
 IccMax=53A  
 Icc\_Dyn=43A  
 Icc\_TDC=36A  
 R\_LL=1.9m ohm  
 OCP=65A

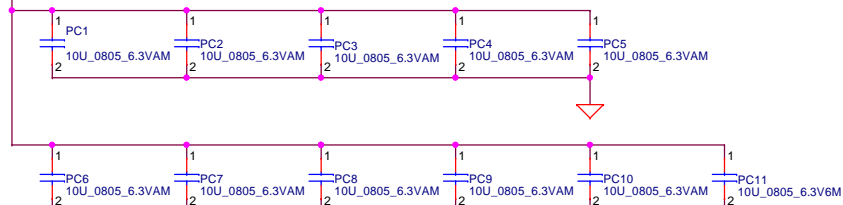


DC 35W GT2  
 VID1=1.23V  
 IccMax=33A  
 Icc\_Dyn=20.2A  
 Icc\_TDC=21.5A  
 R\_LL=3.9m ohm  
 OCP=40A

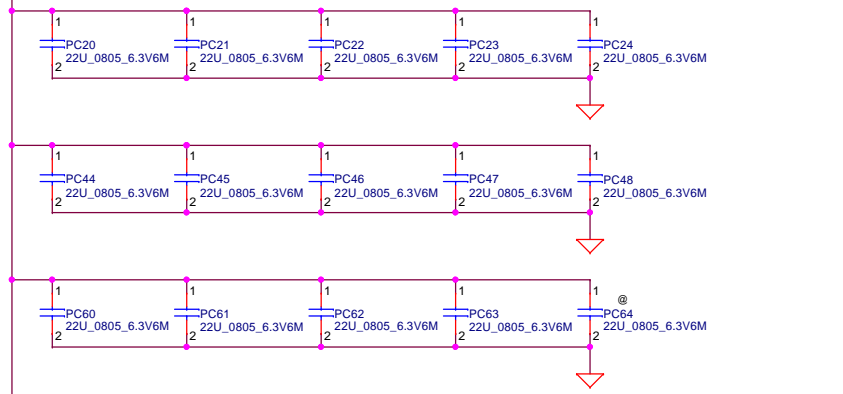
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2012/07/11	Title
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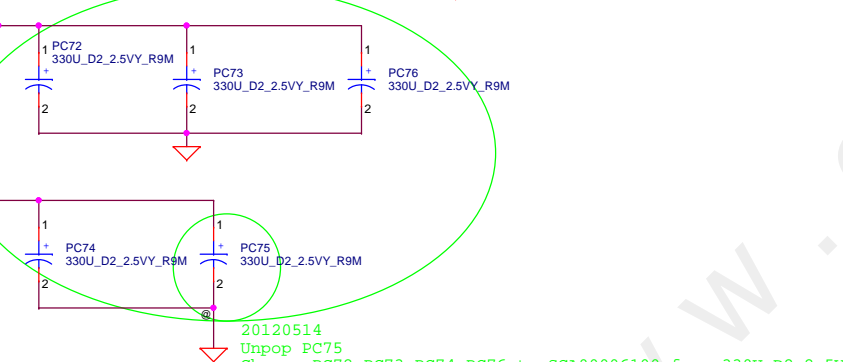
**+VCC\_CORE**



**+VCC\_CORE**

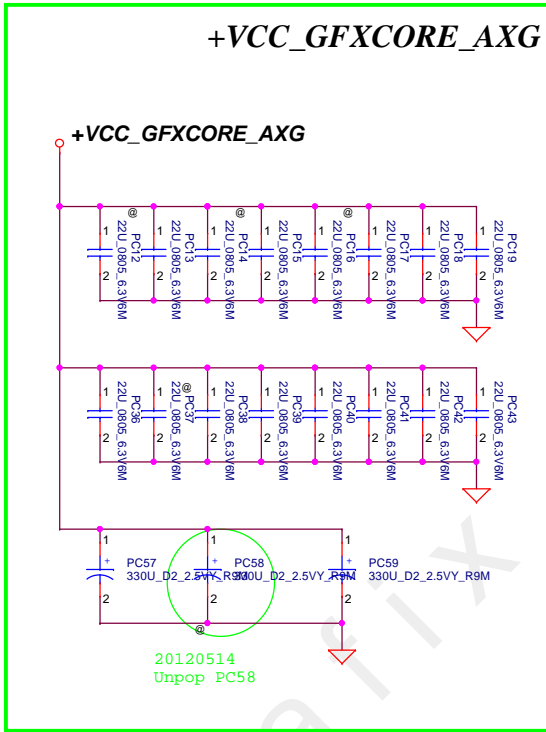


**+VCC\_CORE**



20120318  
Change PC72,PC73,PC74,PC75 to 2 pin footprint  
20120514  
Unpop PC75  
Change PC72,PC73,PC74,PC76 to SGA00006100 from 330U\_D2\_2.5VY\_R9M SGA00002680

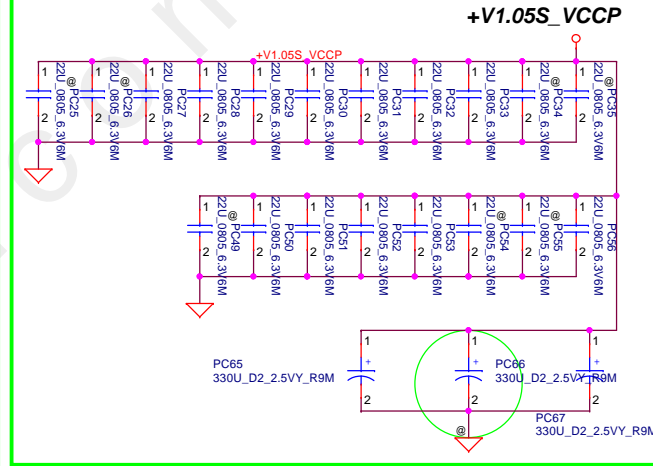
**+VCC\_CORE**



20120514  
Unpop PC58

Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



20120514  
Unpop PC66

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Version change list (P.I.R. List)



Item	Reason for change	PG#	Modify List	Date	Phase
1	For EC net name	P48	PR206 change pull high voltage to +EC_VCCA from +3VLP	20120316	EVT
2	Intersil advise	P54	1.Change PR848 to 1.47K SD000009480 from 1.15K 2.Unmount PC864	20120316	EVT
3	VGA IMON setting	P54	Change PR853 to 11K SD034110280 from 11.3K	20120316	EVT
4	set OCP is 56A	P54	Change PR869 to 1.58K (SD000005J80) from 1K	20120316	EVT
5	For 1.5V current	P51	Add PJ507 for 1.5V	20120321	EVT
6	For B+ layout	P55 P50 P51 P50	1.Change PC954 pull high to CPU_B+ from B+ 2.Change 3/5VALWP B+ input netname to CPU_B+ 3.Change 1.5VALWP B+ input netname to CPU_B+ 4.Change PR411 netname to CPU_B+ from B+	20120321	EVT
7	For HW net name	P53 P54	1.Change +1.05S_VCCP netname to +V1.05S_VCCP 2.Change PQ802.5 netname to +V1.05S_VCCP from +1.05VS	20120330	EVT
8	For HW power sequence	P54	1.Add control PU801 pin GPU_PWR_EN and reserve PR956 0_0402_5% 2.Change PR820 to SD034150380 150K_0402_1% from 100K 3.Change PC810 to SE071101J80 100P_0402_50V8J from 0.1u	20120330	EVT
9	For Intersil advise	P54	Change PR853 pull down netname to gnd	20120409	EVT
10	For IMON design	P55	Change PU901 to NCP6132A from ISL95836	20120412	EVT
11	For layout design	P54	1.Del PJ803 PJ804 2.Change net name to VGACORE from VGACOREP	20120511	DVT
12	For 1.05V, GFX_CORE,CPU_CORE design fine tune	P57	Unpop PC58, PC66,PC75 330U_D2_2.5VY_R9M SGA00002680	20120514	DVT
13	For CPU_CORE design fine tune and ON advise	P57	Change PC72,PC73,PC74,PC76 to S POLY C 330U 2V M D2 ESR9M SGA00006100 from 330U_D2_2.5VY_R9M SGA00002680	20120514	DVT
14	For CPU_CORE design fine tune and ON advise	P55	1.Change PC928 to 560P_0402_50V7K SE074561K80 from 680P_0402_50V7K SE074681K80 2.Change PR949,PR951 to 140K from 130K 3.Change PR912 to 71.5K_0603_1% SD014715280 from 63.4K_0603_1% SD014634280 4.Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE from SL200000500 220K_0402_5%_ERTJOEV224J	20120514	DVT
15	For material EOL	P55	Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE from SL200000500 220K_0402_5%_ERTJOEV224J	20120514	DVT
16	For HW VGA power sequence	P54	Add PR972 SD028000080 0_0402_5% Unmount PD801 Change PR820 to 0_0402_5% SD028000080 from 150K_0402_1% SD034150380 Unmount PC810	20120516	DVT

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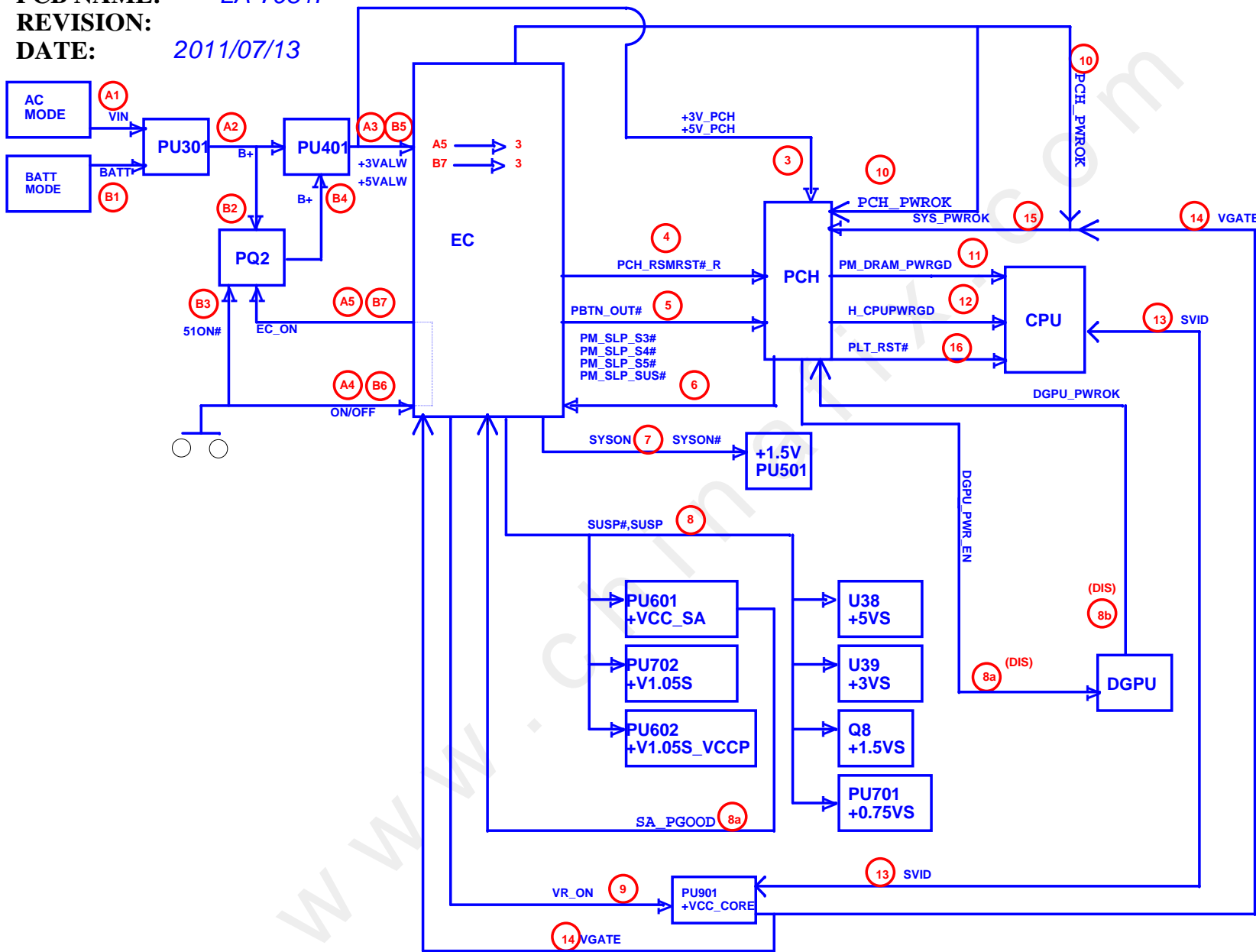


Item	Reason for change	PG#	Modify List	Date	Phase
17	For HW reset function	P50	1.Add PR420 SD028000080 0_0402_5% for reserve 2 reserve.PR419 and PR420	20120606	PVT
18	For ACDET function	P49	1.Change PR313 to 60.4K_0603_1% SD014604280 from 64.9K_0603_1% SD014649280	20120615	PVT
19	For HW Grenn clock UMA sku trial tun	P47	1. unmount PD103 2. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080 Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080	20120625	PVT
20	For ACDET function	P49	1.Change PR313 to 59K_0603_1% SD014590280 from 60.4K_0603_1% SD014604280	20120705	PVT
21	For VR_HOT	P55	1.unmount PR915 and PR946	20120705	PVT
22	For HW Grenn clock	P47	1. mount PD103 2. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080 Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080	20120723	SVT
23	For material issue	P51	1.Change PU502 to SA00004CY10 S IC RT8061AZQW WDFN 10P PWM from SA00003RU00 S IC SY8033BDBC DFN 10P SINGLE BUCK	20120723	SVT

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# COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*  
 PCB NAME: *LA-7981P*  
 REVISION:  
 DATE: *2011/07/13*



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Item	Reason for change	PG#	Modify List	Date	Phase
1	Initial				EVT
2	For LVDS backlight PWM	P33	R431 change from 0ohm_short to 0ohm mount	5/7	EVT
3	For Change Audio Woofer MOSFET from Dual to single channel	P15	Changer Part from SB00000EO10 to SB00000EN00	5/7	EVT
4	For OVERT# Glitch issue at Power on status	P23	Add QV9	5/7	EVT
5	For BT&WLAN Combo Card	P36	to modify R897 value from 0 ohm to 1K ohm add BT_DISABLE_F_R on JWLN1.51 add R5580	5/8	DVT
6	For Factory request and cost down LVDS PIN Define	P33	To Modify LVDS PIN Define	5/8	DVT
7	For USB Charger mode control request	P45 P42	To Add PWRSHARE_EN_R on U31.38 To Add EC_PWRSHARE_EN# on U31.74 add R5577 and R5578, delete CHG_ON#	5/8	DVT
8	To change Reset IC G601	P42	to change R4959 value from 200K ohm to 0 ohm add R5579 0 ohm	5/8	DVT
9	Reserved Touch Screen Power Control	P42 P43	add R5581,C1331,R5572,R5583,R5584 and Q156 add EC_TS_ON on U31.66 add +3VS_TS,+3VS_TS_R	5/8	DVT
10	To change Speaker PIN define for ME routing request	P41	SPK_L2+ R1556 net in JSPK1.1 SPK_L1- R1554 net in JSPK1.2 SPK_R1- R1555 net in JSPK1.3 SPK_R2+ R1553 net in JSPK1.4	5/8	DVT
11	for Realtek Vendor recommend	P41	R1123,C1134 close to U50.47 R5582,R1559 and C1135 Close to U73.1 EXT_MIC_R	5/8	DVT
12	for ME request	P39	To Modify H21,H7,H18 PCB Footprint as below H21 from H_3P3 to H_4P6 H7 from H_2P8 to H_3P0 H18 from H_3P3 to H_3P9N	5/8	DVT
13	for LAN Clock be better	P37	change C990 value from 5PF to 0 ohm.	5/9	DVT
14	for Audio Vendor recommend	P43	change JUSB3.11 from GND to +3VS change JUSB3.12 from +3VS to AGND	5/10	DVT
15	for Crystal finetune Capacitor	P43	C180,C181 from 18PF to 12PF	5/16	DVT
16	for DVT Board ID request	P42	R695 from 33K to 18K	5/17	DVT
17	for PVT request	P37	Change Reference from C990 to R5585	5/23	PVT
18	for Surge request	P38	C1325,C1326,C1327 change package from 0402 to 0603	5/23	PVT
19	for Reset IC function	P42, P50,P43	add R612,PR420,R4960,R4961 Delete R4959	5/24	PVT

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				LA-9603P	1.0
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Version change list (P.I.R. List)



Item	Reason for change	PG#	Modify List	Date	Phase
20	modify N14P_GV2 GPU power sequence	P18	Remove R5575,connect DGPU_PWR_EN to U31.pin89	11/13	PVT
		P46	Add diode D60;D61		
		P46	add discharge(Q157) for DGPU_PWR_EN		
21	for GC6 function	P23	Change RV54 from 10K to 100k	11/29	PVT
22	for GC6 function	P46	Add a 0 ohm R5597 between Q129 pin 2 and Q130 pin	12/26	Pre-MP
23	due to they are cap not resistor.	P46	R1108,R1112 location change to C1108,C1112	12/26	Pre-MP

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				Custom	Document Number
Date:				Wednesday, January 09, 2013	Sheet 62 of 62