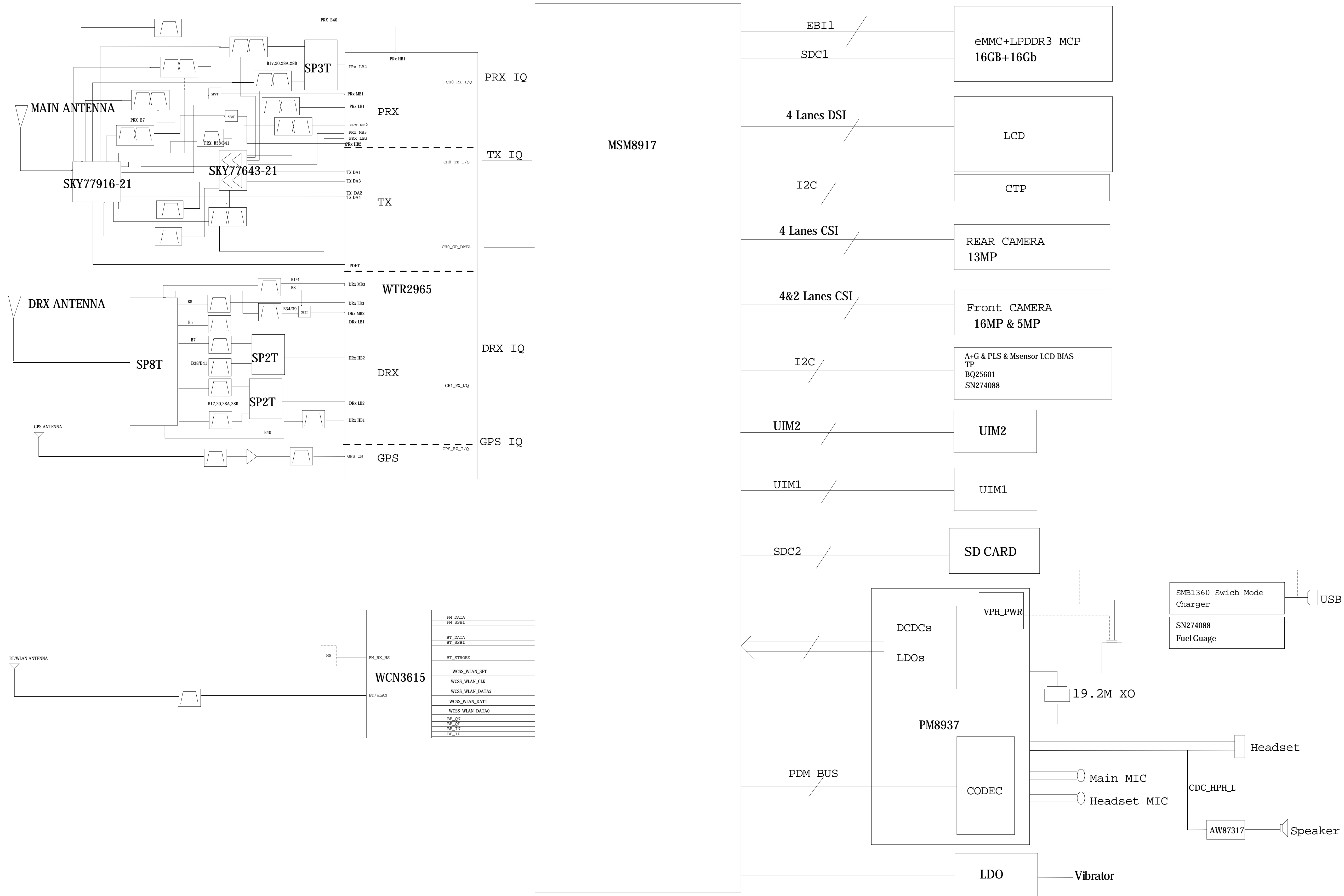


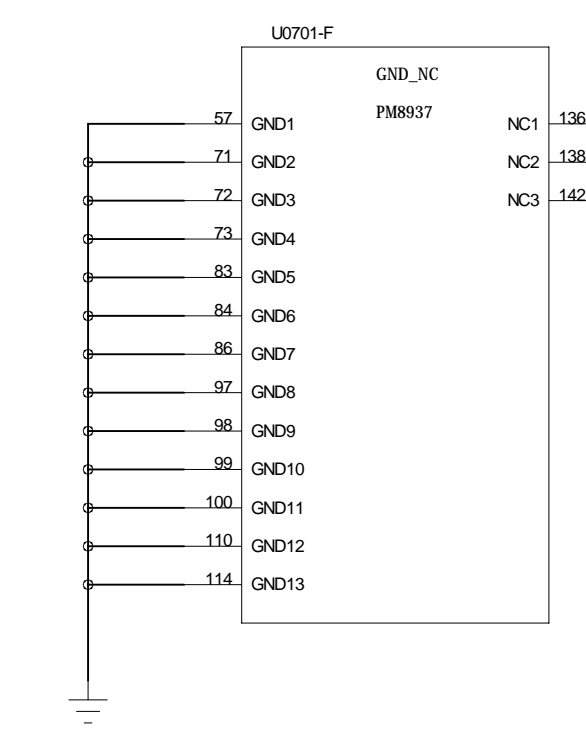
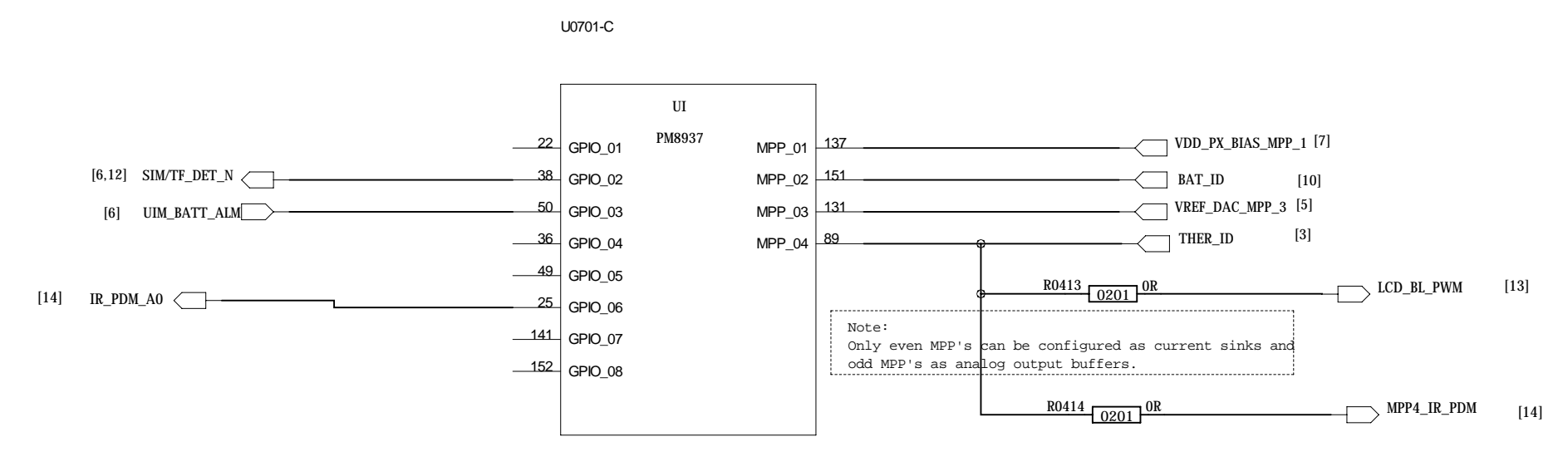
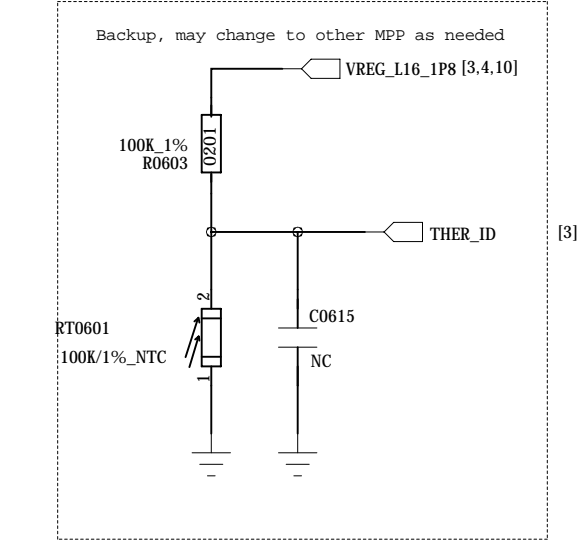
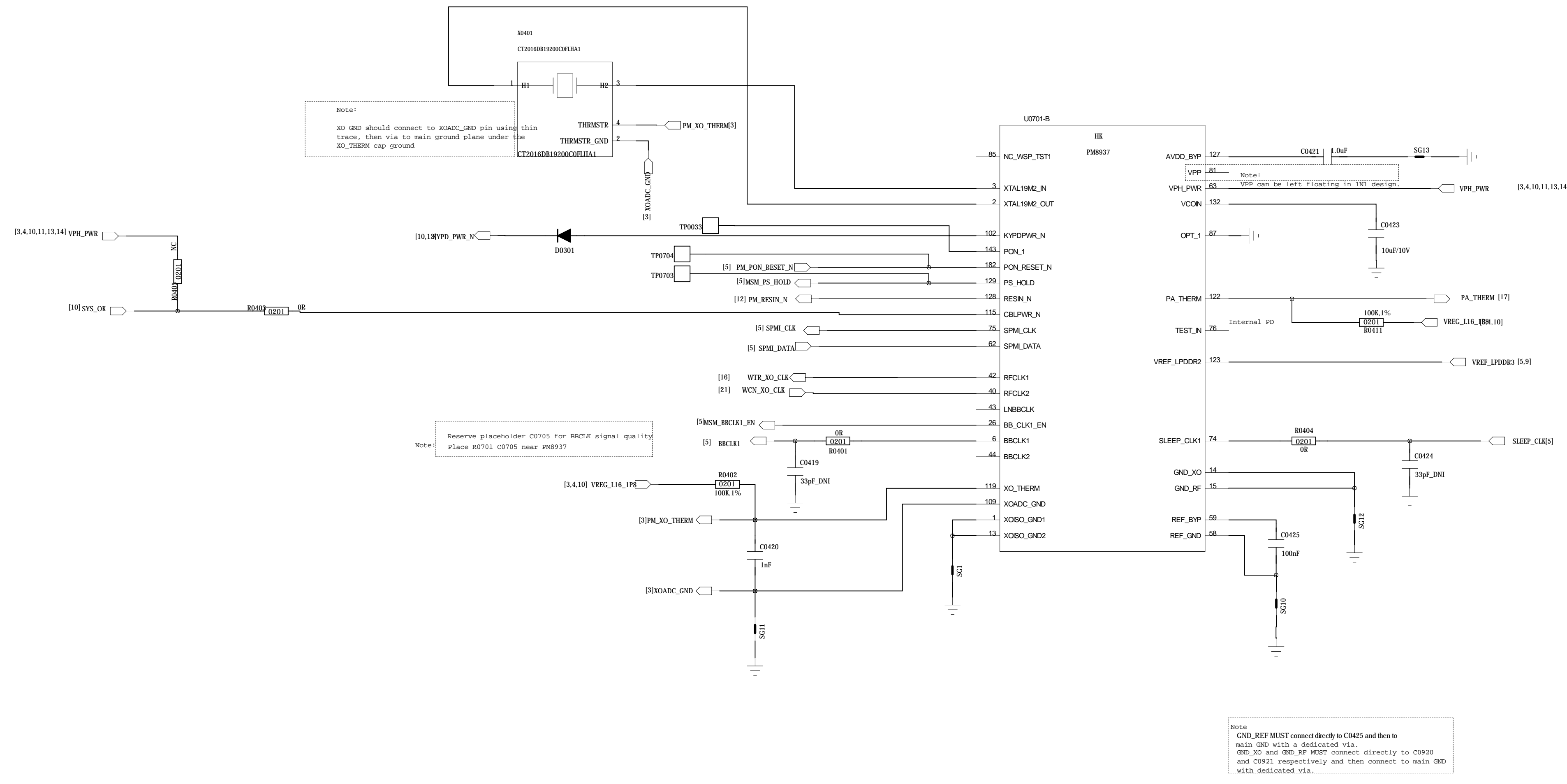
NOTES:MSM8917 GPIO Please refer to the soft to hardware document

GPIO_0	IR_PDM_A0	GPIO_41	DBB2HALL_SEL	GPIO_82	WCSS_FM_DATA
GPIO_1	EXT_AUDIO_PA_RST	GPIO_42	ACCL_INT1_N	GPIO_83	WCSS_BT_CTRL
GPIO_2	LCM_PWM	GPIO_43	ALSP_INT_N	GPIO_84	WCSS_BT_DATA
GPIO_3	NC	GPIO_44	MAG_DRDY_INT	GPIO_85	BISP7_SPI_MO
GPIO_4	UART_MSM_TX	GPIO_45	GYRO_INT_N	GPIO_86	BISP7_SPI_MI
GPIO_5	UART_MSM_RX	GPIO_46	ANT_CHECK	GPIO_87	BISP7_SPI_CSB
GPIO_6	CHARGE_I2C_SDA	GPIO_47	CTP_3V1_EN	GPIO_88	BISP7_SPI_CK
GPIO_7	CHARGE_I2C_SCL	GPIO_48	GPIO_CHAGER_CE	GPIO_89	NC
GPIO_8	MOSI_IR_PDM_A0	GPIO_49	UIM_BATT_ALM	GPIO_90	NC
GPIO_9	VIB_EN	GPIO_50	FLASH_FRONT_EN	GPIO_91	KEY_VOL_UP_N
GPIO_10	TP_I2C_SDA	GPIO_51	UIM1_DATA	GPIO_92	NC
GPIO_11	TP_I2C_SCL	GPIO_52	UIM1_CLK	GPIO_93	GPIO_LCM_LED_EN
GPIO_12	LCM_ENP	GPIO_53	UIM1_RESET	GPIO_94	BOARD_ID0
GPIO_13	LCM_ENN	GPIO_54	SIM/TF_DET_N	GPIO_95	BOARD_ID1
GPIO_14	SENSOR_I2C_SDA	GPIO_55	UIM2_DATA	GPIO_96	NC
GPIO_15	SENSOR_I2C_SCL	GPIO_56	UIM2_CLK	GPIO_97	NC
GPIO_16	GPIO_KEY_LED_EN	GPIO_57	UIM2_RESET	GPIO_98	SCAM_DVDD_EN
GPIO_17	TP_ID	GPIO_58	SIM/TF_DET_N	GPIO_99	SCAM_AVDD_EN
GPIO_18	LED_I2C_SDA	GPIO_59	LCM_ID0	GPIO_100	RFFE1_CLK
GPIO_19	LED_I2C_SCL	GPIO_60	LCD_RST_N	GPIO_101	RFFE1_DATA
GPIO_20	BOARD_ID2	GPIO_61	SMB_INT	GPIO_102	RFFE2_CLK
GPIO_21	BOARD_ID3	GPIO_62	GAUGE_INT	GPIO_103	RFFE2_DATA
GPIO_22	LDCBIAS_I2C_SDA	GPIO_63	NC	GPIO_104	DRX_B3_B39_SW
GPIO_23	LDCBIAS_I2C_SCL	GPIO_64	TP_RST_N	GPIO_105	PRX_B1_B4_SW
GPIO_24	LCD_TED	GPIO_65	TP_INT_N	GPIO_106	PRX_MB2_B3_B34_B39_SW1
GPIO_25	DPDT_SWITCH_EN	GPIO_66	LCM_ID1	GPIO_107	PRX_MB2_B3_B34_B39_SW2
GPIO_26	CAM_MCLK0	GPIO_67	SIM/TF_DET_N	GPIO_108	PRX_B7_B38_B41_SW
GPIO_27	CAM_MCLK1	GPIO_68	NC	GPIO_109	DRX_ANT_SW1
GPIO_28	NC	GPIO_69	CDC_PDM_CLK	GPIO_110	DRX_ANT_SW2
GPIO_29	CAM_I2C_SDA0	GPIO_70	CDC_PDM_SYNC	GPIO_111	FBRX_SEL
GPIO_30	CAM_I2C_SCL0	GPIO_71	CDC_PDM_TX	GPIO_112	DRX_HB2_B7_B38_B41
GPIO_31	CAM_I2C_SDA1	GPIO_72	CDC_PDM_RX0	GPIO_113	NC
GPIO_32	CAM_I2C_SCL1	GPIO_73	CDC_PDM_RX1	GPIO_114	DBB2RF_TUNER_VC7
GPIO_33	GPIO_FLASH_EN	GPIO_74	CDC_PDM_RX2	GPIO_115	DBB2RF_TUNER_VC8
GPIO_34	GPIO_FLASH_STROBE	GPIO_75	WCSS_BT_SSB1	GPIO_116	NC
GPIO_35	NC(MCAM_PWDN)	GPIO_76	WCSS_WLAN_DATA_2	GPIO_117	NC
GPIO_36	MCAM_RST_N	GPIO_77	WCSS_WLAN_DATA_1	GPIO_118	EXT_GPS_LNA_EN
GPIO_37	FORCE_USR_BOOT	GPIO_78	WCSS_WLAN_DATA_0	GPIO_119	CHO_GSM_TX_PHASE_D0
GPIO_38	HALL2DBB_INT	GPIO_79	WCSS_WLAN_SET	GPIO_120	RFFES_CLK
GPIO_39	NC(SCAM_PWDN)	GPIO_80	WCSS_WLAN_CLK	GPIO_121	RFFES_DATA
GPIO_40	SCAM_RST_N	GPIO_81	WCSS_FM_SSB1	GPIO_125	NC
GPIO_123	NC	GPIO_124	EINT_FTP	GPIO_122	NC
GPIO_126	NC	GPIO_127	NC	GPIO_128	GPIO_FP_ID0_EN
GPIO_129	GPIO_WHITE_EN	GPIO_130	NC	GPIO_131	NC
GPIO_132	GPIO_FP_RST	GPIO_133			

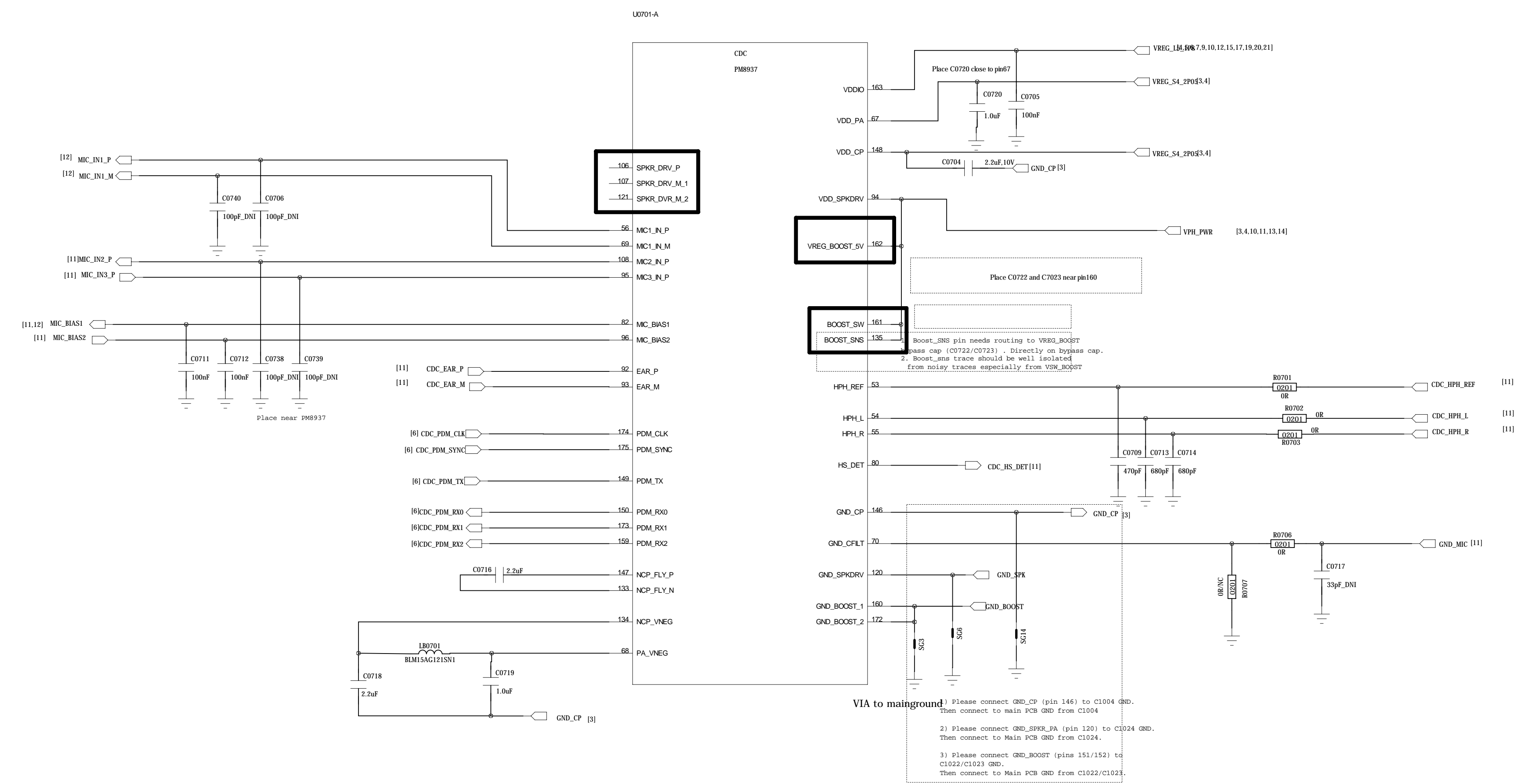


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SCALE: <Scale>				SHEET 2/1 21			

PM8937 CONTROL



PM8937 CODEC



VIA to mainground
 1) Please connect GND_CP (pin 140) to G104 GND. Then connect to main PCB GND from G104.
 2) Please connect GND_SPMODV (pin 126) to G104 GND. Then connect to main PCB GND from G104.
 3) Please connect GND_BOOST (pin 151/152) to G104 GND. Then connect to main PCB GND from G104/G103.

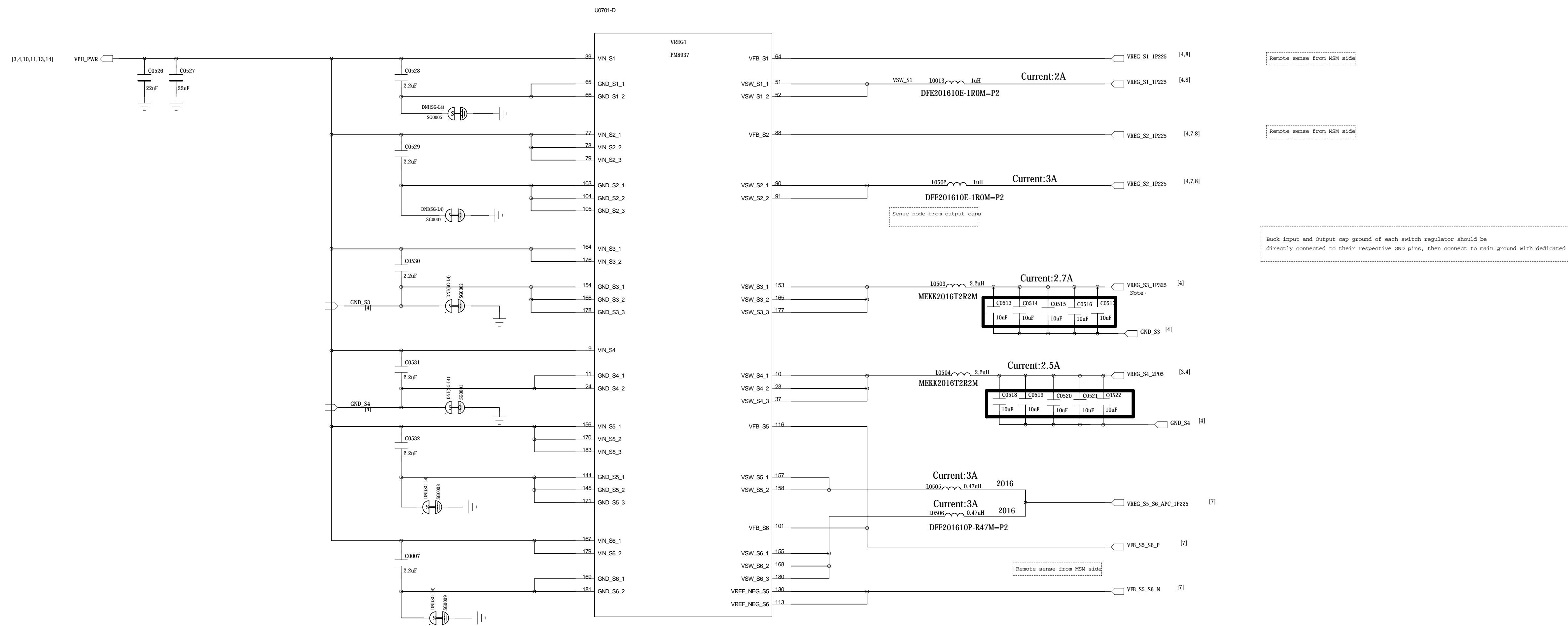
COMPANY: Shanghai Longcheer Technology Co., Ltd

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SHEET: 3 of 21			

DRAWN: LAY/BBB
 CHECKED: YaoGang

BUCK

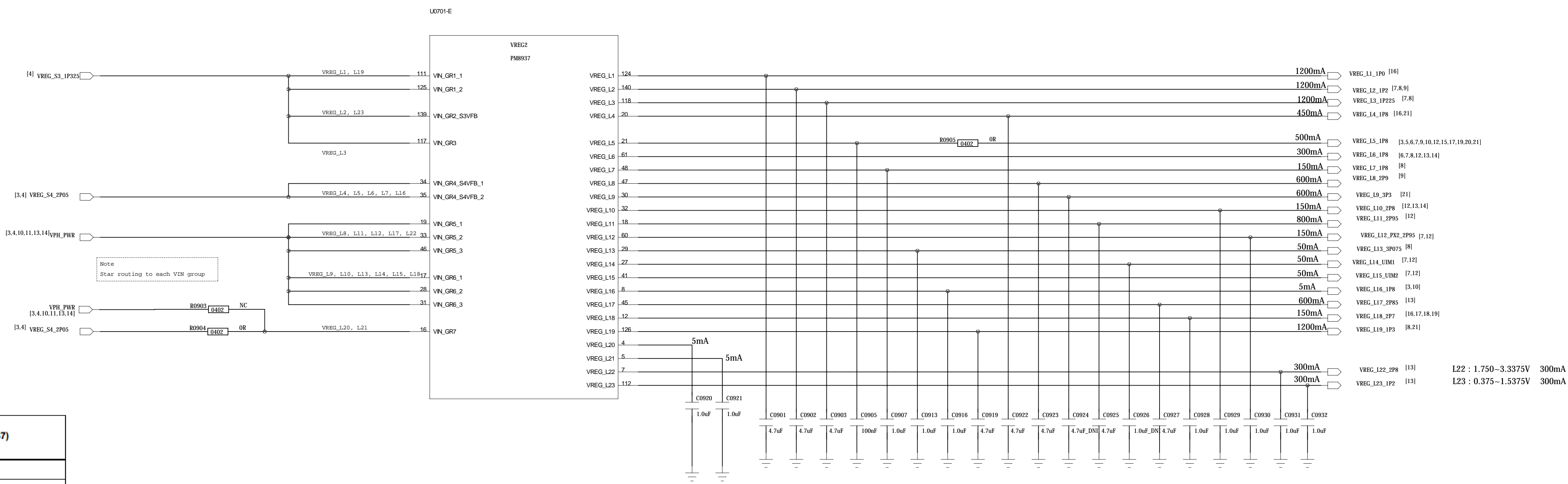


Remove sense from HSN side

Remove sense from HSN side

Both input and output tap ground of each switch regulator should be directly connected to their respective GND pins, then connect to main ground with dedicated vias

LDO



PSEUDO CAPLESS LDOs
 L4*, L6, L8*, L9*, L10, L11*, L12, L14, L15, L17*, L18, L22, L23
 L4*, L8*, L9*, L11*, L17*, still need validation as Pseudo-capless
 L5, L7, L13, L16 have internal PMIC Loads and require local CAPs.

Table 3-6 PM8937/PM8940 regulators and their intended uses

Function	Circuit type	Default V (V) ¹	Specified range (V) ² (MSM8937)	Programmable range (V)	Rated current (mA)	Default on	Expected use (MSM8937)
S1	ULT-SMPS	1.225	0.900-1.350	0.375-1.5625	2000 ³	N	MSM modem
S2	ULT-SMPS	1.225	0.550-1.350	0.375-1.5625	3000	Y	MSM core and graphics
S3	HF-SMPS	1.288	1.200-1.4125	0.375-1.5625	2700	Y	Low-voltage LDOs (1, 2, 3, 19, and 23)
S4	ULT-SMPS	2.050	1.800-2.050	1.550-3.125	2500	Y	High-voltage LDOs (4, 5, 6, 7, 16, RFCLK, and XO)
S5	FT-SMPS	1.225	1.050-1.350	0.350-1.355	3000	Y	MSM applications processor
S6	FT-SMPS	1.225	1.050-1.350	0.350-1.355	3000	N	MSM applications processor
L1	NMOS LDO	1.000	1.000	0.375-1.5375	1200	N	RFICs
L2	NMOS LDO	1.200	1.200	0.375-1.5375	1200	Y	LPDDR2/LPDDR3, MIPI CSI, and DSI
L3	NMOS LDO	1.225	0.750-1.350	0.375-1.5375	1200	Y	VDDMX
L4	PMOS LDO	1.800	1.800	1.750-3.3375	450	N	RFICs and GPS eNANA
L5 ⁴	PMOS LDO	1.800	1.600	1.750-3.3375	500	Y	Most digital ICs, MSM pad groups 3 and 7, LPDDR, and eMMC
L6	PMOS LDO	1.800	1.800	1.750-3.3375	300	N	MSM DSI PLL and OTP, camera, touchscreen, display, and sensors
L7	PMOS LDO	1.800	1.800	1.750-3.3375	150	Y	MSM analog and PLLs, WCN XO, and PM baseband clock driver
L8	PMOS LDO	2.900	2.900	1.750-3.3375	600	Y	eMMC
L9	PMOS LDO	$V_{out} = 3.3V$ for $V_{BAT} > 3.575V$, $V_{out} = 3V$ for $V_{BAT} < 3.575V$	3.000-3.300	1.750-3.3375	600	N	WCN
L10	PMOS LDO	2.8	2.800	1.750-3.3375	150	N	Sensors
L11 ⁵	PMOS LDO	2.950	2.950	1.750-3.3375	800	Y	Micro SD
L12 ⁴	PMOS LDO	2.950	1.800/2.950	1.750-3.3375	150	Y	MSM pad group 2 and SDC2
L13	PMOS LDO	3.075	3.075	1.750-3.3375	50	Y	MSM USB and audio

COMPANY: Shanghai Longcheer Technology Co., Ltd

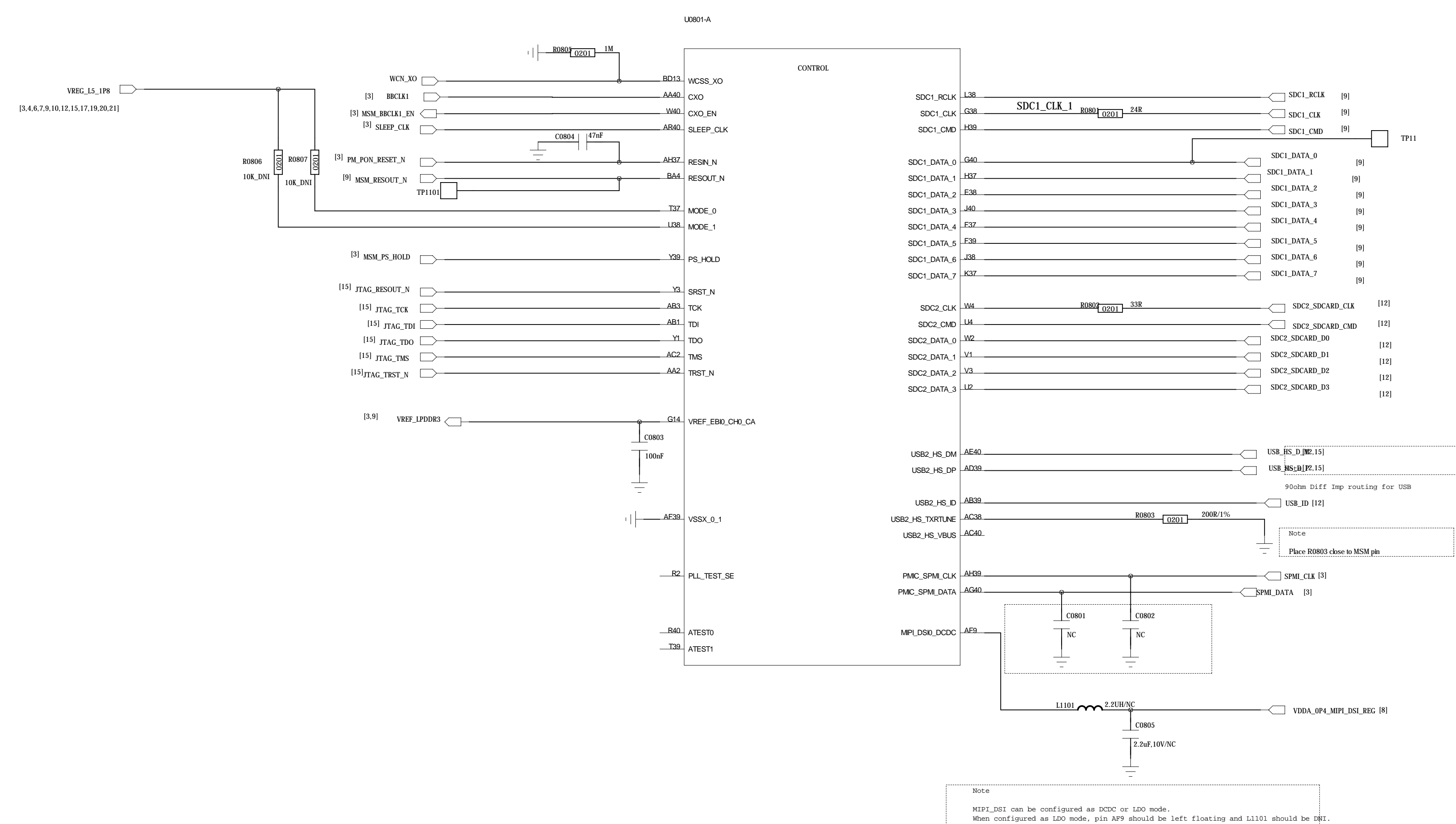
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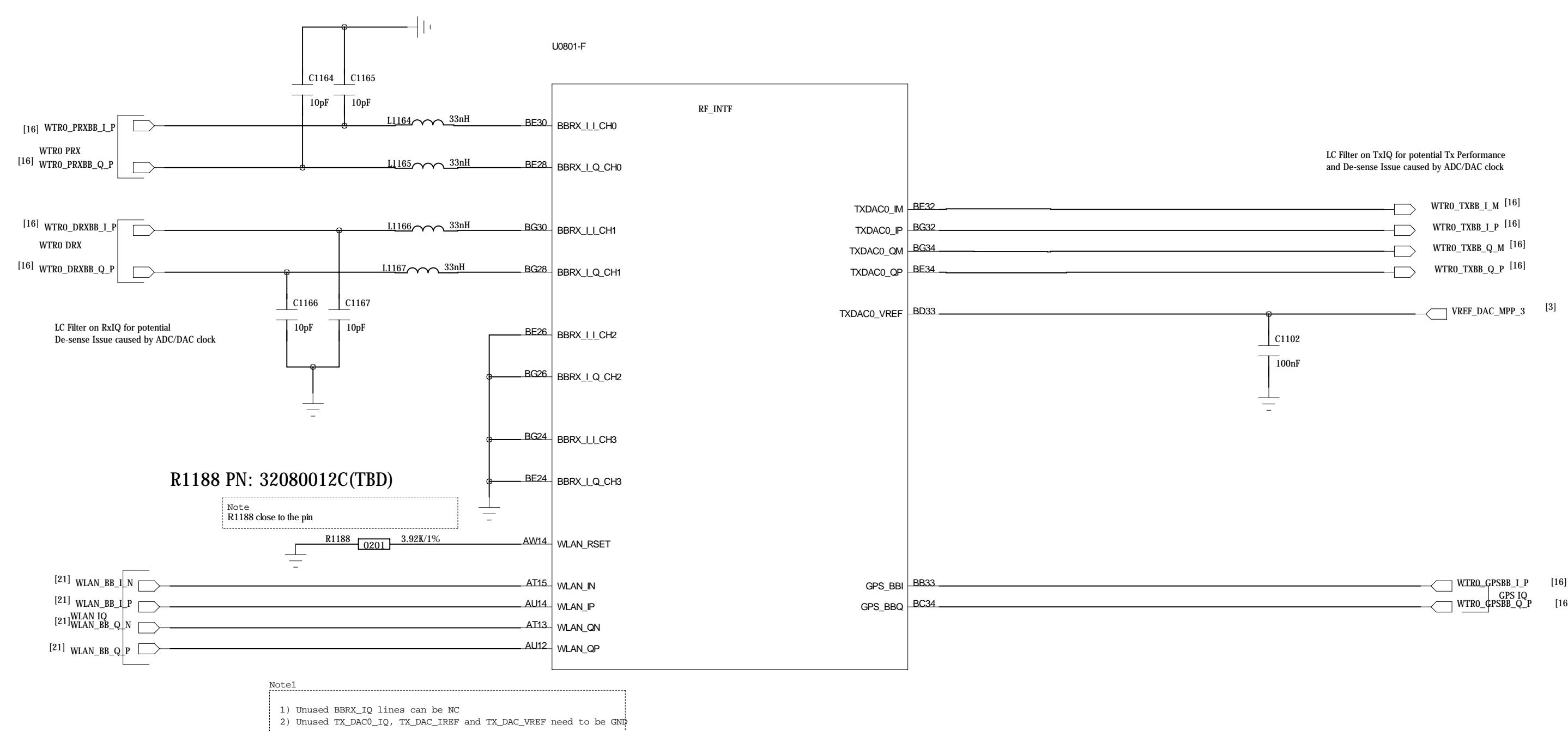
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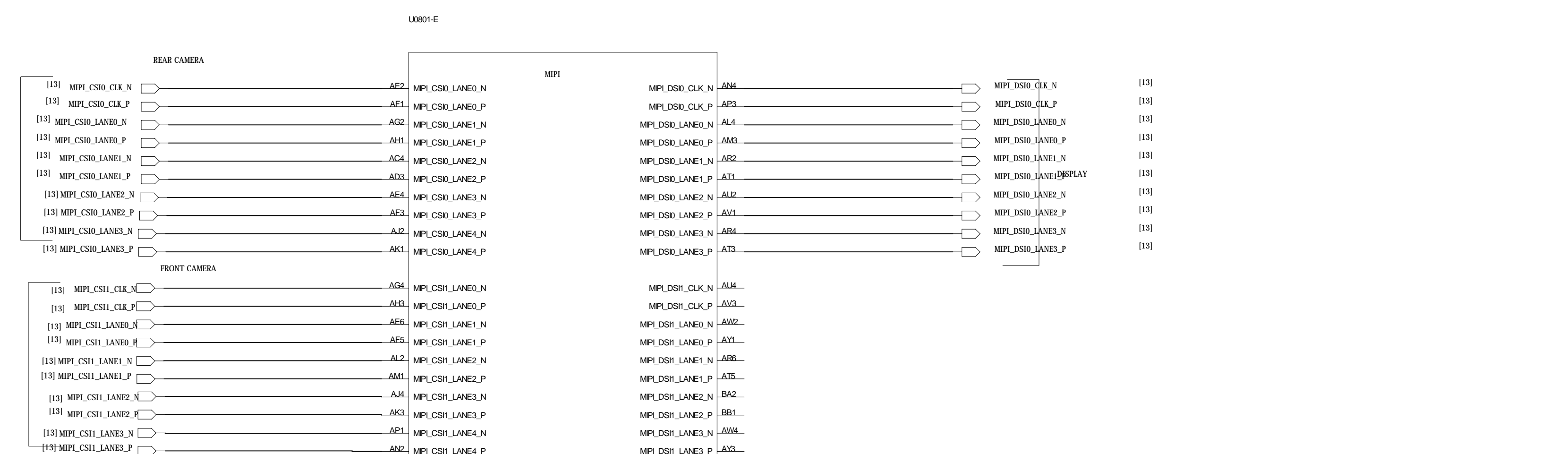
MSM8937_CONTROL



RF_CONTROL



MSM8937_MIPI



Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints. Extreme care must be taken that no stubs are created by doing so.

MSM8937_EBI

