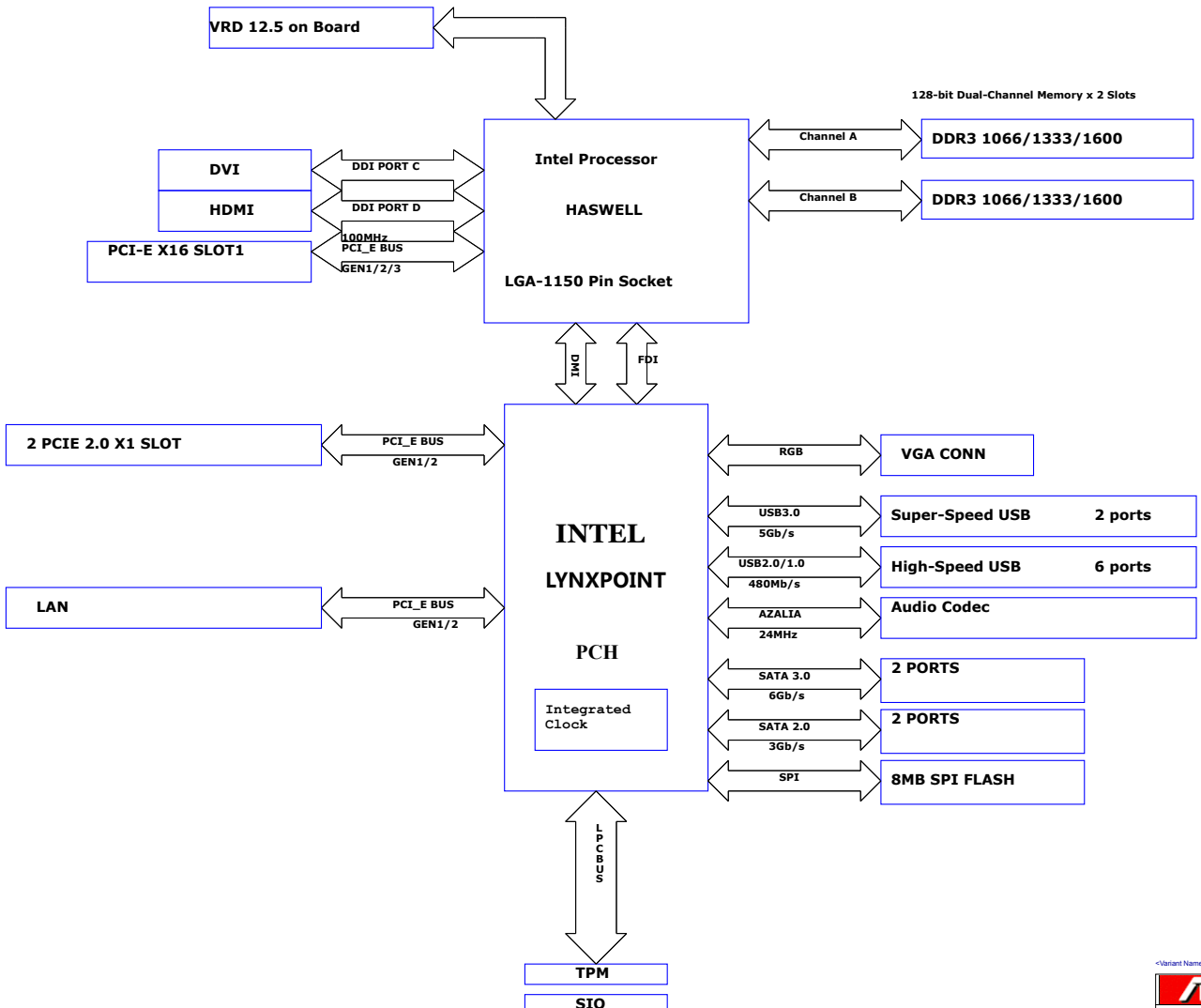
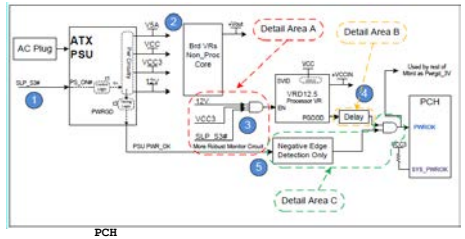


<Variant Name>

ASUS	Title :	BLOCK DIAGRAM
<OrgName>	Engineer:	key_cai
Size: A3	Project Name: Standard Circuit	Rev: 0.03A
Date: Monday, July 14, 2014	Sheet 1 of 65	



PCH
LYNX POINT

PCI_Express x 16_1 — PWRGD — <19>O_PCIRST#_PCIEX16_1
PCI_Express x 16_2 — PWRGD — <19>O_PCIRST#_PCIEX16_2
PCI_Express x 1_1,2 & xI6_3 — PWRGD — <19>O_PCIRST#_PCIEX16_3

POWER_SWITCH
PWRBTN
HIGHMAT

SIO
NCT6779D

<5>O_PWRBTN#IN
PS_IN#
PCIRST1#
PCIRST2#
PCIRST3#
LRESET#
KBRST#
RSMRST#
PS_OUT#
SUSC#
SUSB#
PSON#
ATXPGD
PWROK

<18>S_PLTRST#
O_KB_RST#
<4>O_RSMRST#
<6>O_PWRBTN#
<4.1> / <8>S_SLPS4#
<4.2> / <9>S_SLPS3#
<7>S_SLP_A#

POWER SUPPLY
Main PWR
VSB
PSON#
PWROK
<2>AC Power Switch On
<10>12V,5V,3V
<3>+5VSB, +3VSB
<9>O_PSON#
<11>B_ATX_PWROK

HDA_RST#
AZ_RST#
RESET#
AUDIO
ALC898
SYS_RESET#
PLTRST#
PLTRST_PROC#
RCIN#
DRAMPWROK
RSMRST#
RTCRST#
PWRBTN#
SRTCRST#
SLP_S5#
SLP_S4#
SLP_S3#
PROCPUPWRGD
SLP_A#
SLP_LAN#
DPWROK
SYS_PWROK
PCH_PWROK
MEPWROK

<1>RTCRST#
<1>SRTCRST#
BATTERY
<3.1>S_DPWROK
<12>O_PWROK
fast boot
+3V delay 99ms
Non-AMT
AMT

ME_POWER
+1.05ME
+3V_EPW
<7.2>S_MEPWROK

RESET_SWITCH
XDP
SYS_RESET#
H_CPURST#
DBR#
RESET#
OBSDATA

PROCESSOR
HASWELL
DBR#
RESET#
SM_DRAMPWROK
CFG
<18>H_CPURST#
<13>S_DRAMPWRGD
<14>H_CPUPWRGD
PWRGOOD
SVID
VCORE
<15>VRM_SVID
<16>VCORE

Vcore Controller
SVID
VCORE
VR_ON
PGOOD
ISL95818
<17>VRMPWRGD
S_SLPS3#
+12V
+3V

*1 PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#

*2 PWROK will assert when +3V arrives at +2.1V then delay 300ms~500ms and gated by ATXPGD

*3 If support AMT, SLP_A# could already be high before sequence begins. If not support AMT, SLP_A# will come with SLP_S3

*4 SLP_S4# controls +1.5VDual and +VTTDDR

*5 Come with 1.5VDUAL

*6 Come with +3V,+12V and gated by SLP_S3#

*7 CPUPWRGD= After PWROK

*8 PLTRST# = PCH PWROK AND PCH SYS_PWROK

*9 PLTRST_PROC#=PLTRST#, voltage=1V, directly connect to CPU

CHIP
SOCKET or SLOT

<Variant Name>
ASUS
Title : POWER SEQUENCE
<OrgName>
Engineer: key_cai
Size A3
Project Name Standard Circuit
Rev 0.03A
Date: Monday, July 14, 2014
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