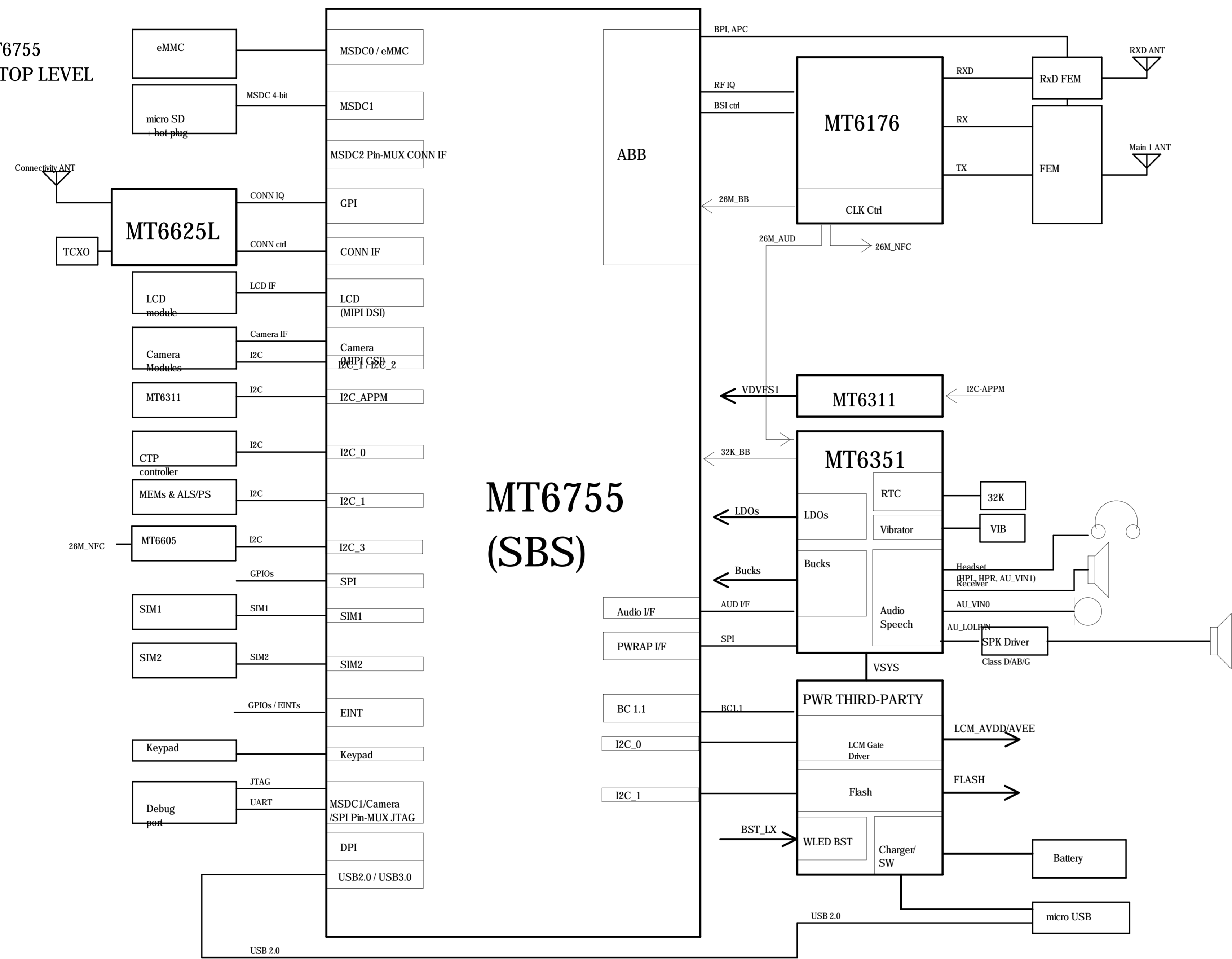


REVISION HISTORY			
REV	ECO NO.	APPROVED	DATE

Project : MT6755
REF_SCH TOP LEVEL



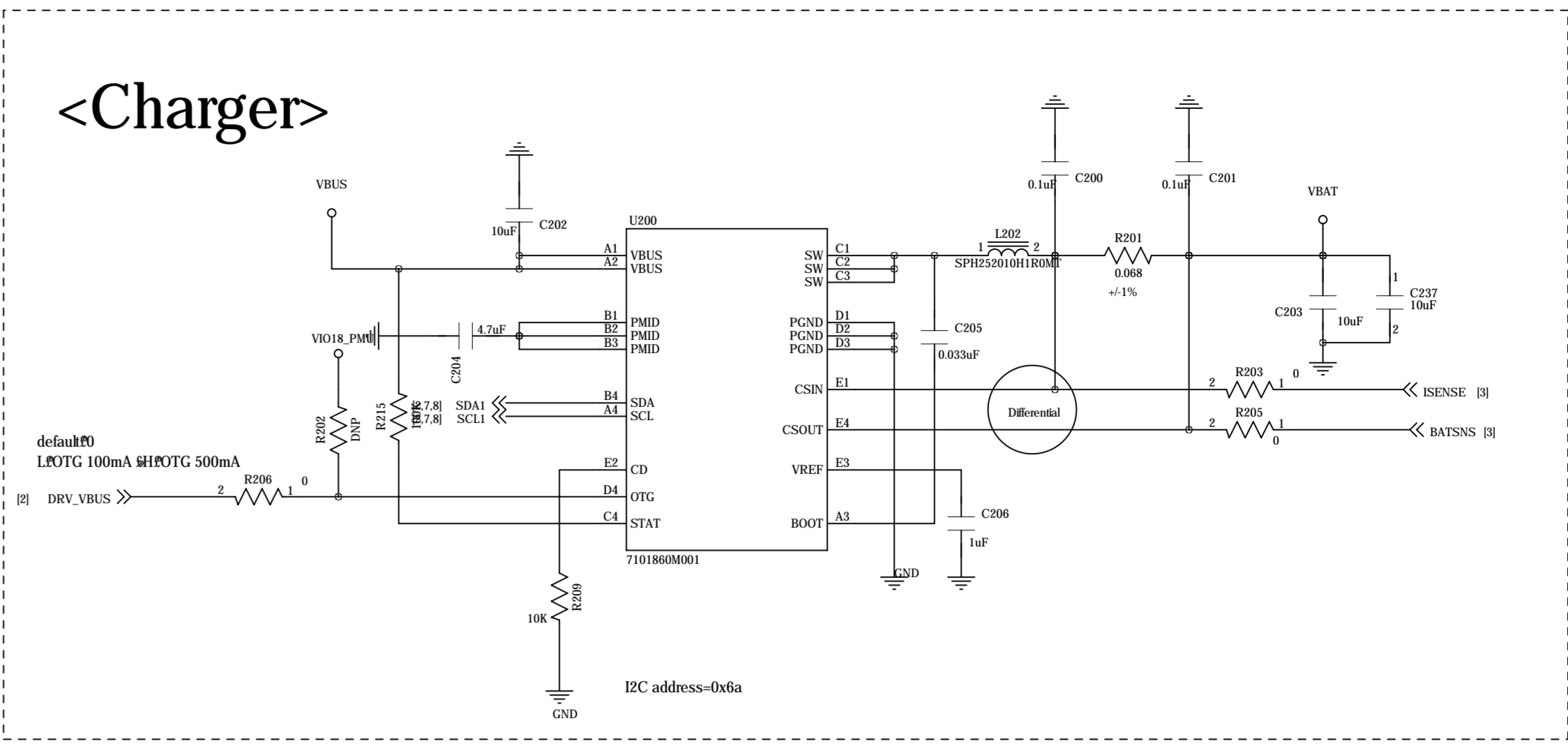
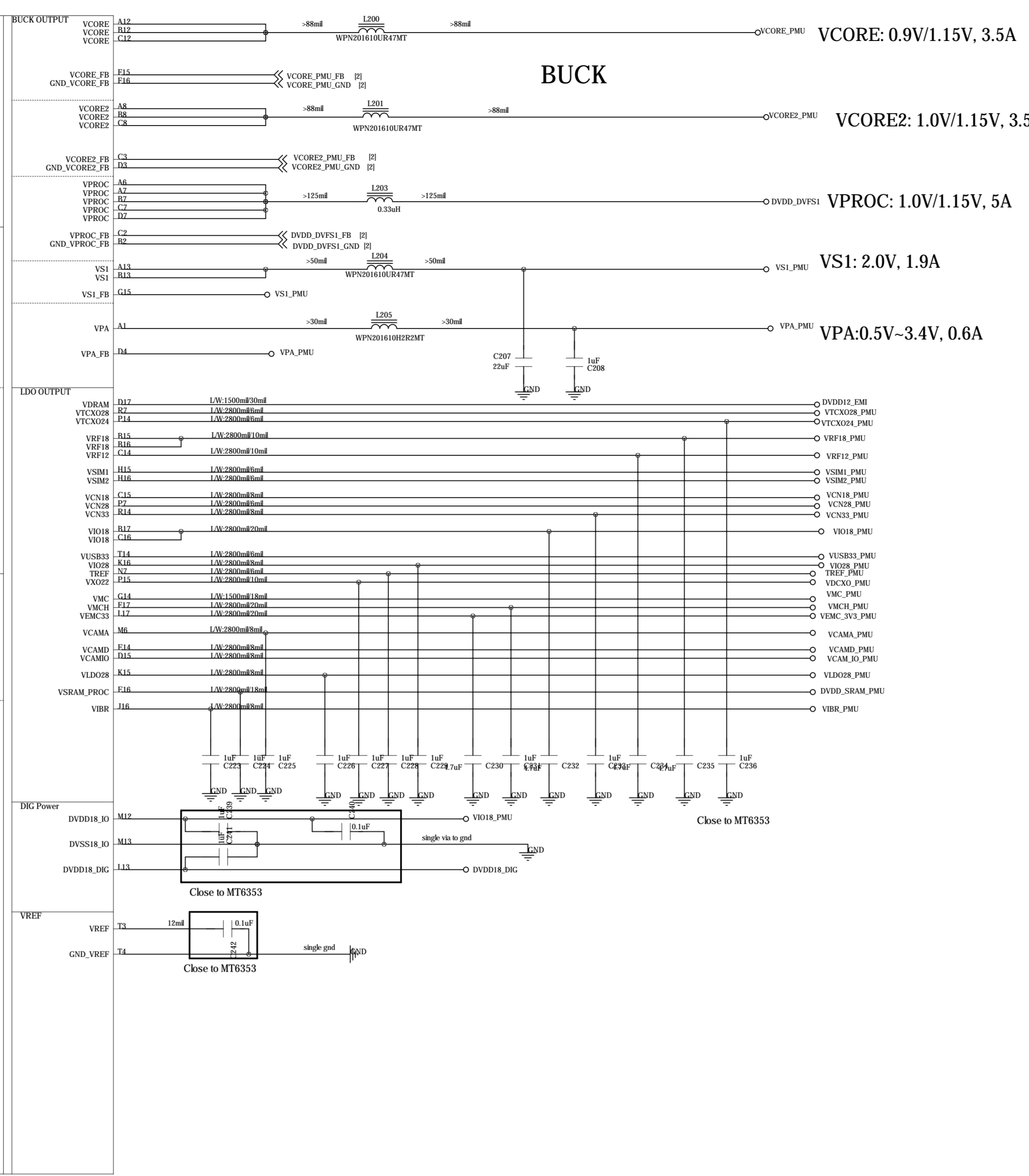
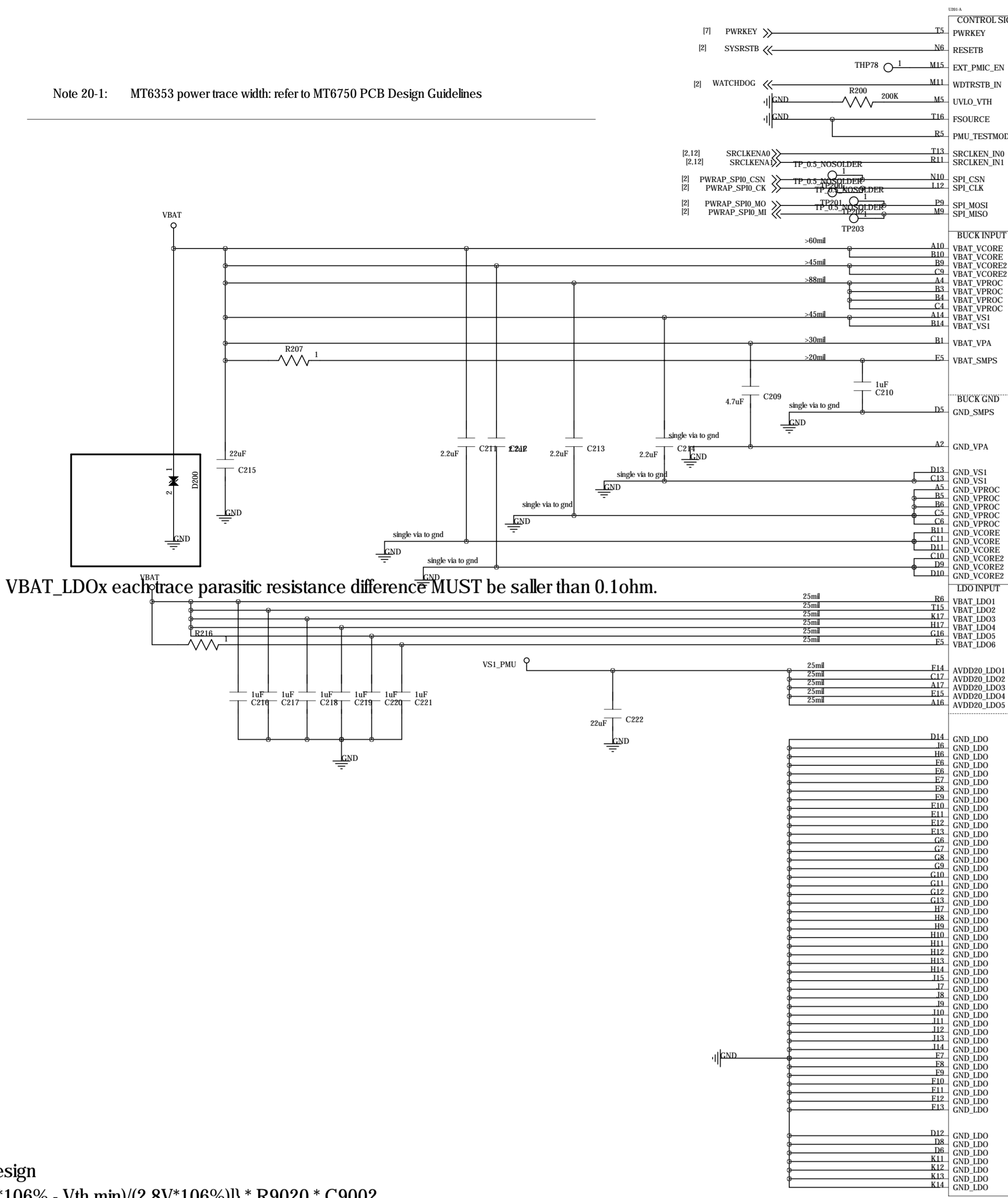
I2C	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)
I2C-0	CTP	400 Kbps	Yes.	GT1151 I2C address: 0X5D (Write:0x8A, Read:0xBB) or 0x14 (Write:0x28, Read:0x29)
	LCM Gate Driver	400 Kbps		NT50358 / LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)
I2C-1	M Sensor	400 Kbps		YAS533 / M-Sensor I2C Address: 0x2E (Write: 0x5C, Read: 0x5D)
	A+Gyro Sensor	400 Kbps	Yes.	MPU-6515 / A-Gyro I2C Address: 0x68 (Write:0xD0, Read:0xD1)
	Baro Sensor	400 Kbps		BMP280 / Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)
	RGB / PS Sensor	400 Kbps		CM36558/ RGB+PS I2C address: 0x51 (Write:0xTBC, Read:0xTBC)
	Flash LED	400 Kbps		RT4505 / Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)
	Front Camera - 8M	400 Kbps	Yes.	Front camera (OV8858) I2C address: 0X10 (Write:0x20, Read:0x21) AF driver (BU64245GWZ) I2C address: 0X0C (Write:0x18, Read:0x19)
I2C-2	Rear Camera - 16M	400 Kbps	Yes.	Rear camera (S5K2P8) I2C address: 0X10 (Write:0x20, Read:0x21) AF driver (BU64297GWZ-TR) I2C address: 0X0C (Write:0x18, Read:0x19)
I2C-3	NFC	1.2 Mbps	Yes.	NFC I2C address: 0X28 (Write:0x50, Read:0x51)
I2C-APPM	MT6311	TBD	Yes.	MT6311 / 2-Phase Buck I2C address: 0X0B (Write:0x, Read:0x)

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

DRAWN		DATED		CODE		SIZE		DRAWING NO.		REV.	
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QUALITY CONTROL		DATED		TITLE							
RELEASED		DATED									

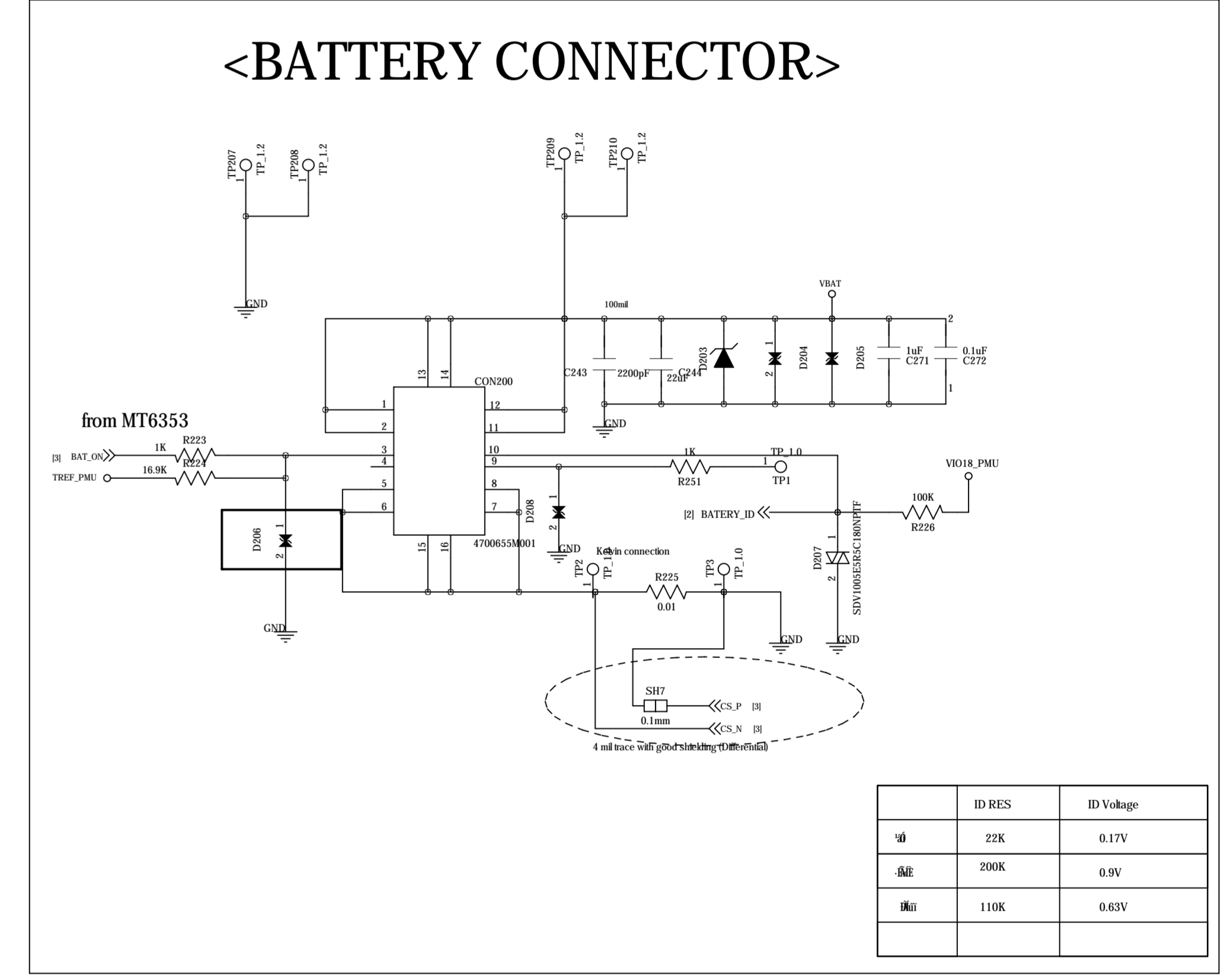
REVISION RECORD			
ITER	ECO NO.	APPROVED	DATE

Note 20-1: MT6353 power trace width: refer to MT6750 PCB Design Guidelines



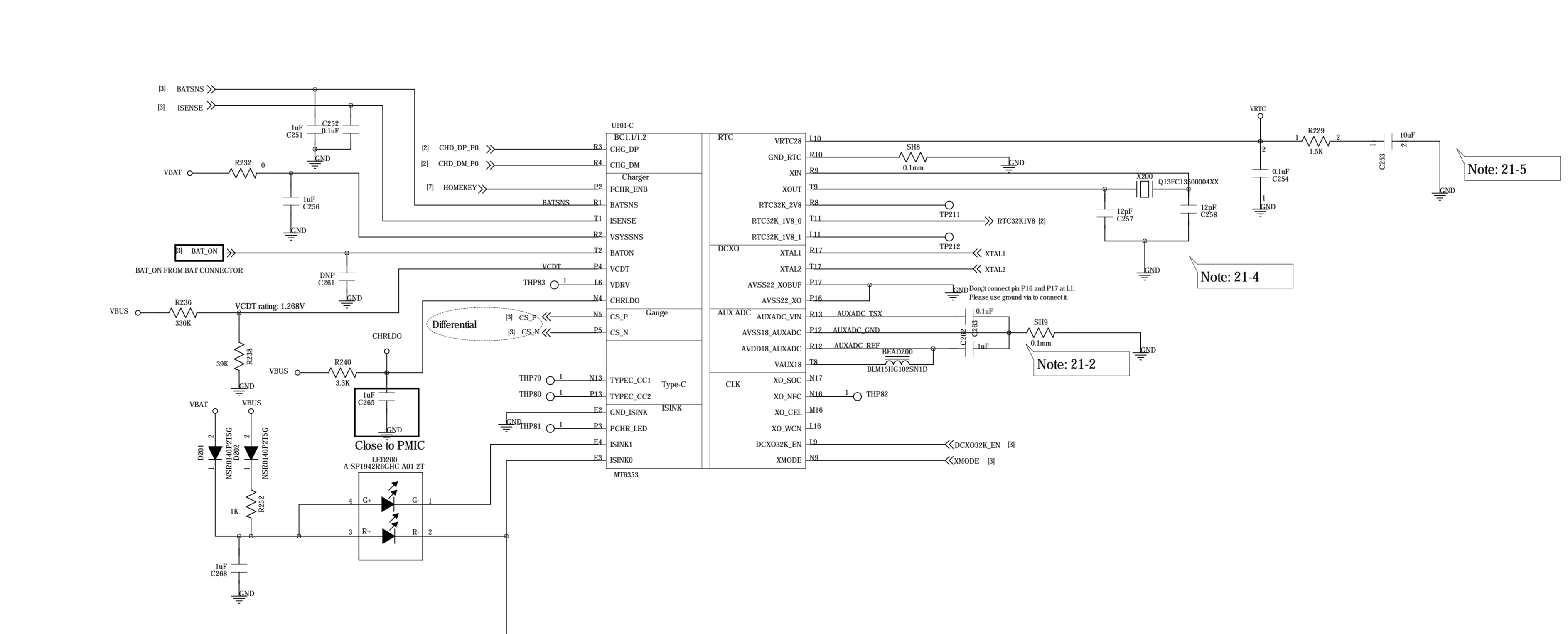
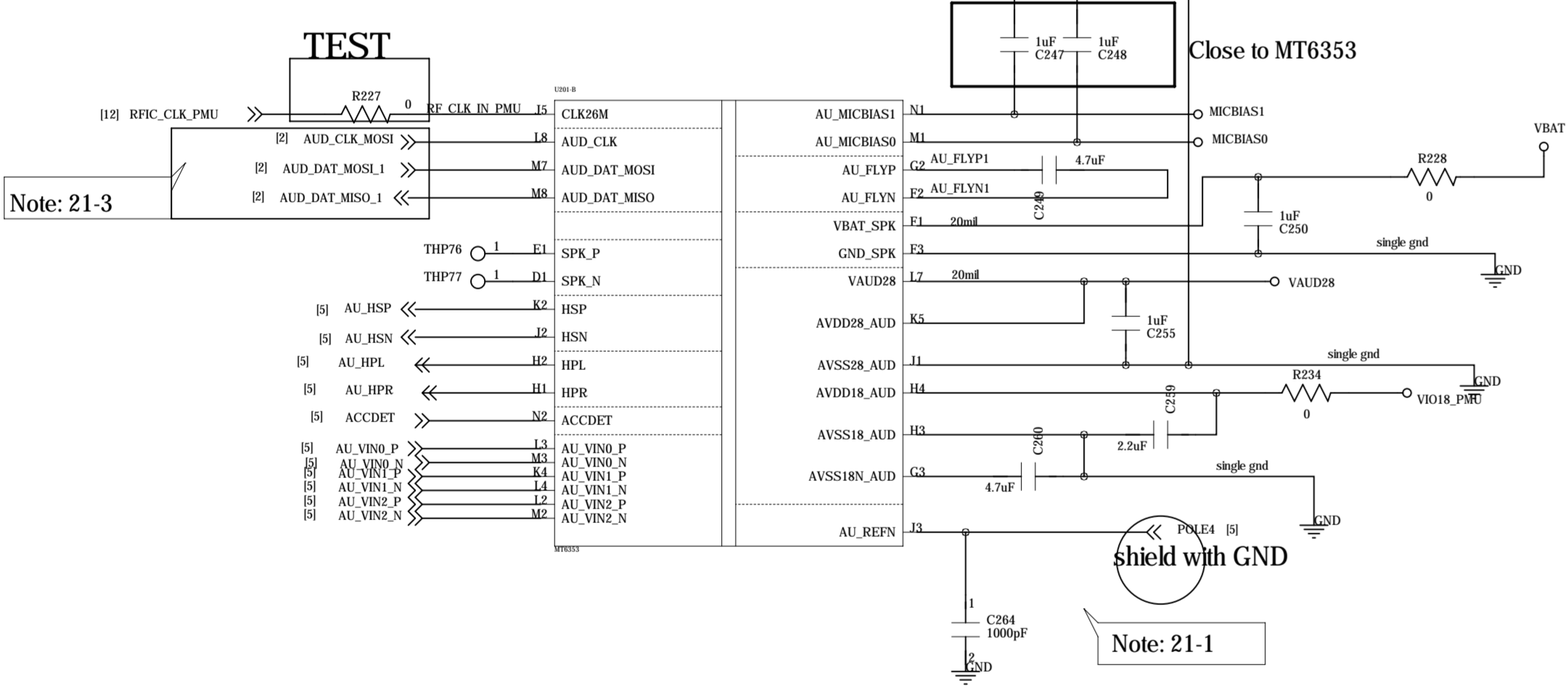
Charger setting

	Internal charger	External charger	
	Pulse charger	Power Path	No Power Path
BATSNS	VBAT	VSYS	VBAT
ISENSE	VBAT(Rsns)	VBAT	VBAT
VSYSNS	VBoost	VBoost	VBoost

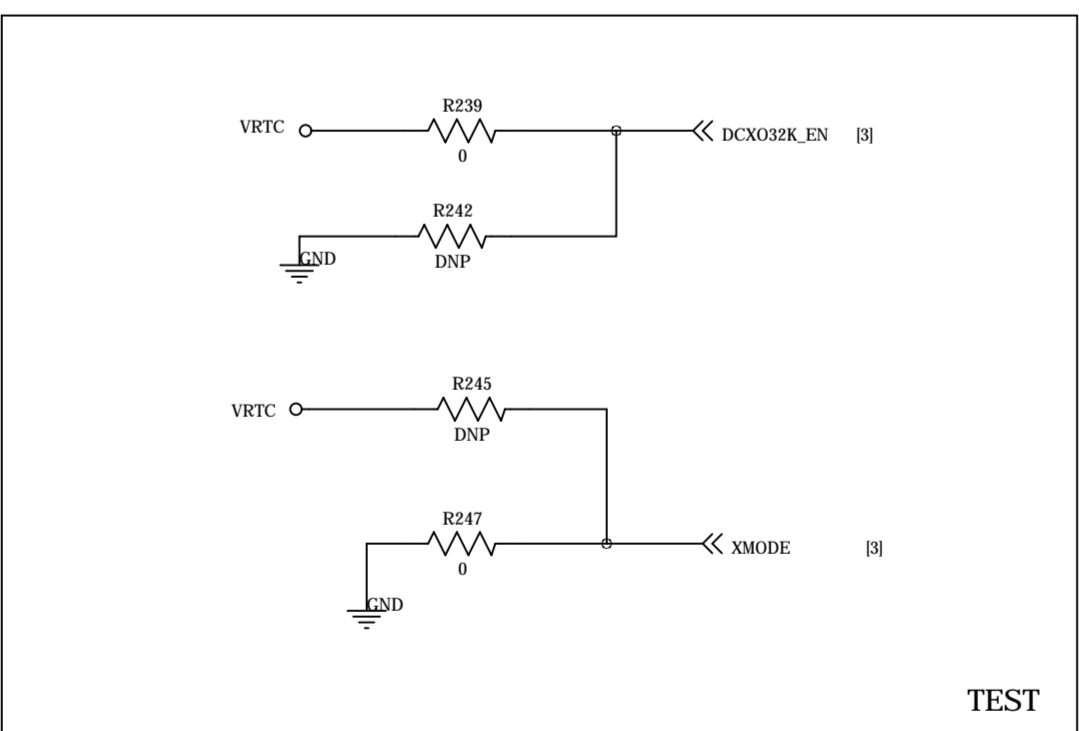


ID RES	ID Voltage
10	21K 0.17V
100	20K 0.9V
10K	10K 0.65V

Delay time design
 $t = -ln [(2.8V * 106\% - V_{th, min}) / (2.8V * 106\%)] * R9020 * C9002$
 where $V_{th, min}$ is minimum turn-on threshold of N-MOS.



DCX032_EN	XMODE	CLK_OUT
1	0	VTCXO on MT6176 (OFF XO in MT6353)
1	1	TSX on MT6353, w/o RTC



Route AUXADC_REF/AUXADC_TSX as differential trace (1 mil each) with GND shielding and route AUXADC_GND with 15mil trace width under AUXADC_TSX/AUXADC_REF trace to provide return current path.

Connect to interface for reserved layout area

- Note 21-1: Layout trace from MT6353 ball 13 AUDREFN to Audio jack GND must surround shield with GND. The AUDREFN pin of MT6353 needs to shunt a noise-decoupling capacitor (typical value is 1nF) to ground in order to minimize FM de-sense. This noise-decoupling capacitor must be placed as close to MT6353 as possible in PCB layout.
- Note 21-2: Route AUXADC_REF/AUXADC_TSX as differential trace (1 mil each) with GND shielding and route AUXADC_GND with 15mil trace width under AUXADC_TSX/AUXADC_REF trace to provide return current path.
- Note 21-3: AUD_CLK_MOSIAUD_DAT_MOSIAUD_DAT_MISO should surround shield with GND. AUD_CLK_MOSIAUD_DAT_MOSIAUD_DAT_MISO layout trace should be same length and cannot over 1350mils.
- Note 21-4:
- Note 21-5:

COMPANY				
TITLE				
DESIGN	DATE:	CODR	REV	DRAWING NO
CHECKED	DATE:			REV
QUALITY CONTROL	DATE:			
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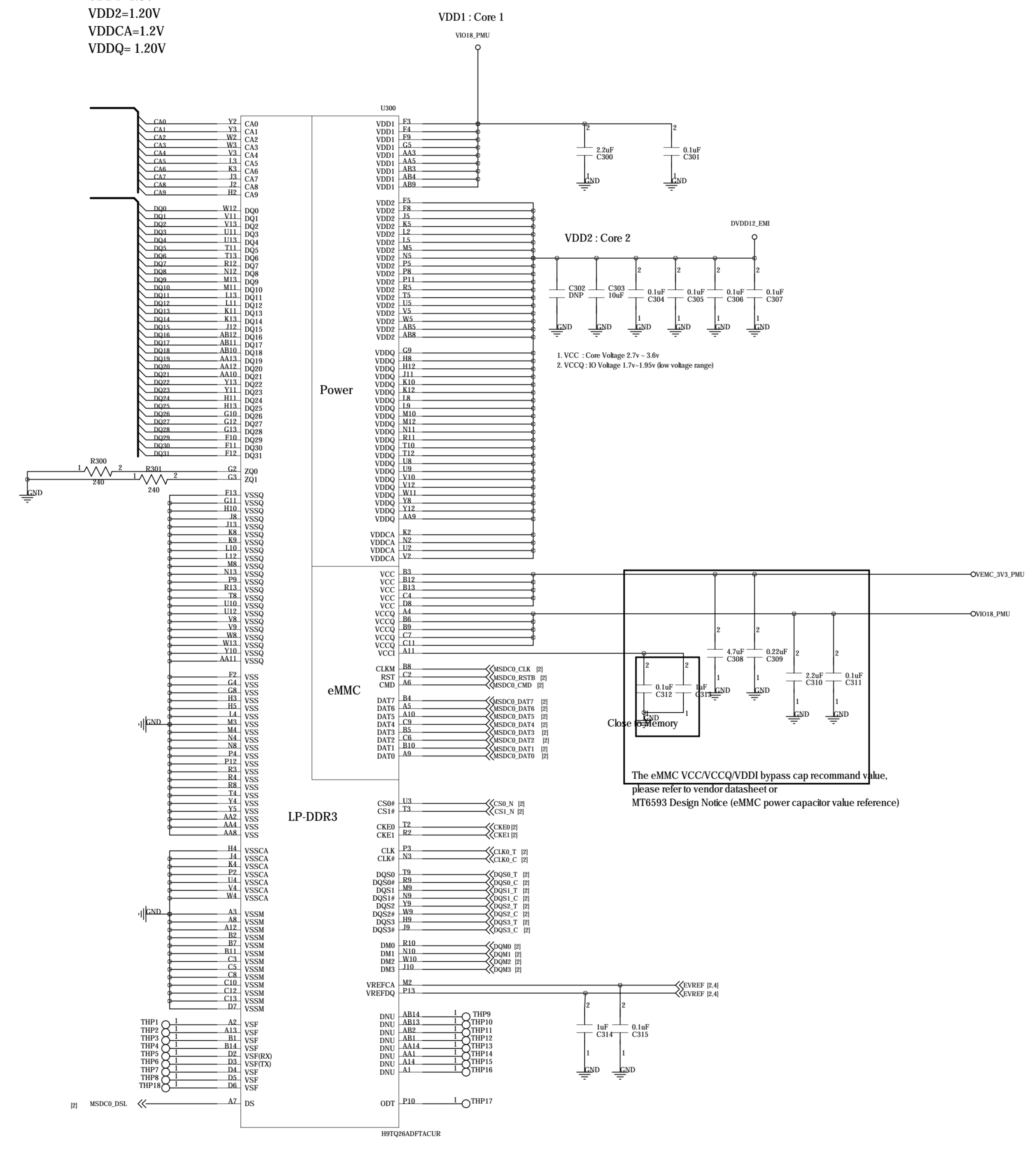
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ITER	ECO NO.	APPROVED	DATE

eMMC+LPDDR3

VDD1=1.8V
VDD2=1.20V
VDDCA=1.2V
VDDQ= 1.20V

Connect to AP	
DQB1_I1	DQB1_I1
CAR_R	CAR_R
CS1_N	CS1_N
CS1_N	CS1_N
CKE	CKE
DQM0	DQM0
DQM1	DQM1
DQOE	DQOE
DQO3	DQO3
DQO3_C	DQO3_C
DQO3_C	DQO3_C
DQO3_C	DQO3_C
DQO3_T	DQO3_T
DQO3_T	DQO3_T
DQO3_T	DQO3_T
CLK0_T	CLK0_T
CLK0_C	CLK0_C
VREF_CA	VREF_CA
VREF_IQ	VREF_IQ
VREF_IQ	VREF_IQ

Power I/F	
VDD1_P0U	VDD1_P0U
VDD1_P1U	VDD1_P1U
VDD1_P2U	VDD1_P2U
VDD1_P3U	VDD1_P3U
VDD1_P4U	VDD1_P4U
VDD1_P5U	VDD1_P5U
VDD1_P6U	VDD1_P6U
VDD1_P7U	VDD1_P7U
VDD1_P8U	VDD1_P8U
VDD1_P9U	VDD1_P9U
VDD1_P10U	VDD1_P10U
VDD1_P11U	VDD1_P11U
VDD1_P12U	VDD1_P12U
VDD1_P13U	VDD1_P13U
VDD1_P14U	VDD1_P14U
VDD1_P15U	VDD1_P15U
VDD1_P16U	VDD1_P16U
VDD1_P17U	VDD1_P17U
VDD1_P18U	VDD1_P18U
VDD1_P19U	VDD1_P19U
VDD1_P20U	VDD1_P20U
VDD1_P21U	VDD1_P21U
VDD1_P22U	VDD1_P22U
VDD1_P23U	VDD1_P23U
VDD1_P24U	VDD1_P24U
VDD1_P25U	VDD1_P25U
VDD1_P26U	VDD1_P26U
VDD1_P27U	VDD1_P27U
VDD1_P28U	VDD1_P28U
VDD1_P29U	VDD1_P29U
VDD1_P30U	VDD1_P30U
VDD1_P31U	VDD1_P31U
VDD1_P32U	VDD1_P32U
VDD1_P33U	VDD1_P33U
VDD1_P34U	VDD1_P34U
VDD1_P35U	VDD1_P35U
VDD1_P36U	VDD1_P36U
VDD1_P37U	VDD1_P37U
VDD1_P38U	VDD1_P38U
VDD1_P39U	VDD1_P39U
VDD1_P40U	VDD1_P40U
VDD1_P41U	VDD1_P41U
VDD1_P42U	VDD1_P42U
VDD1_P43U	VDD1_P43U
VDD1_P44U	VDD1_P44U
VDD1_P45U	VDD1_P45U
VDD1_P46U	VDD1_P46U
VDD1_P47U	VDD1_P47U
VDD1_P48U	VDD1_P48U
VDD1_P49U	VDD1_P49U
VDD1_P50U	VDD1_P50U
VDD1_P51U	VDD1_P51U
VDD1_P52U	VDD1_P52U
VDD1_P53U	VDD1_P53U
VDD1_P54U	VDD1_P54U
VDD1_P55U	VDD1_P55U
VDD1_P56U	VDD1_P56U
VDD1_P57U	VDD1_P57U
VDD1_P58U	VDD1_P58U
VDD1_P59U	VDD1_P59U
VDD1_P60U	VDD1_P60U
VDD1_P61U	VDD1_P61U
VDD1_P62U	VDD1_P62U
VDD1_P63U	VDD1_P63U
VDD1_P64U	VDD1_P64U
VDD1_P65U	VDD1_P65U
VDD1_P66U	VDD1_P66U
VDD1_P67U	VDD1_P67U
VDD1_P68U	VDD1_P68U
VDD1_P69U	VDD1_P69U
VDD1_P70U	VDD1_P70U
VDD1_P71U	VDD1_P71U
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VDD1_P73U	VDD1_P73U
VDD1_P74U	VDD1_P74U
VDD1_P75U	VDD1_P75U
VDD1_P76U	VDD1_P76U
VDD1_P77U	VDD1_P77U
VDD1_P78U	VDD1_P78U
VDD1_P79U	VDD1_P79U
VDD1_P80U	VDD1_P80U
VDD1_P81U	VDD1_P81U
VDD1_P82U	VDD1_P82U
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VDD1_P86U	VDD1_P86U
VDD1_P87U	VDD1_P87U
VDD1_P88U	VDD1_P88U
VDD1_P89U	VDD1_P89U
VDD1_P90U	VDD1_P90U
VDD1_P91U	VDD1_P91U
VDD1_P92U	VDD1_P92U
VDD1_P93U	VDD1_P93U
VDD1_P94U	VDD1_P94U
VDD1_P95U	VDD1_P95U
VDD1_P96U	VDD1_P96U
VDD1_P97U	VDD1_P97U
VDD1_P98U	VDD1_P98U
VDD1_P99U	VDD1_P99U



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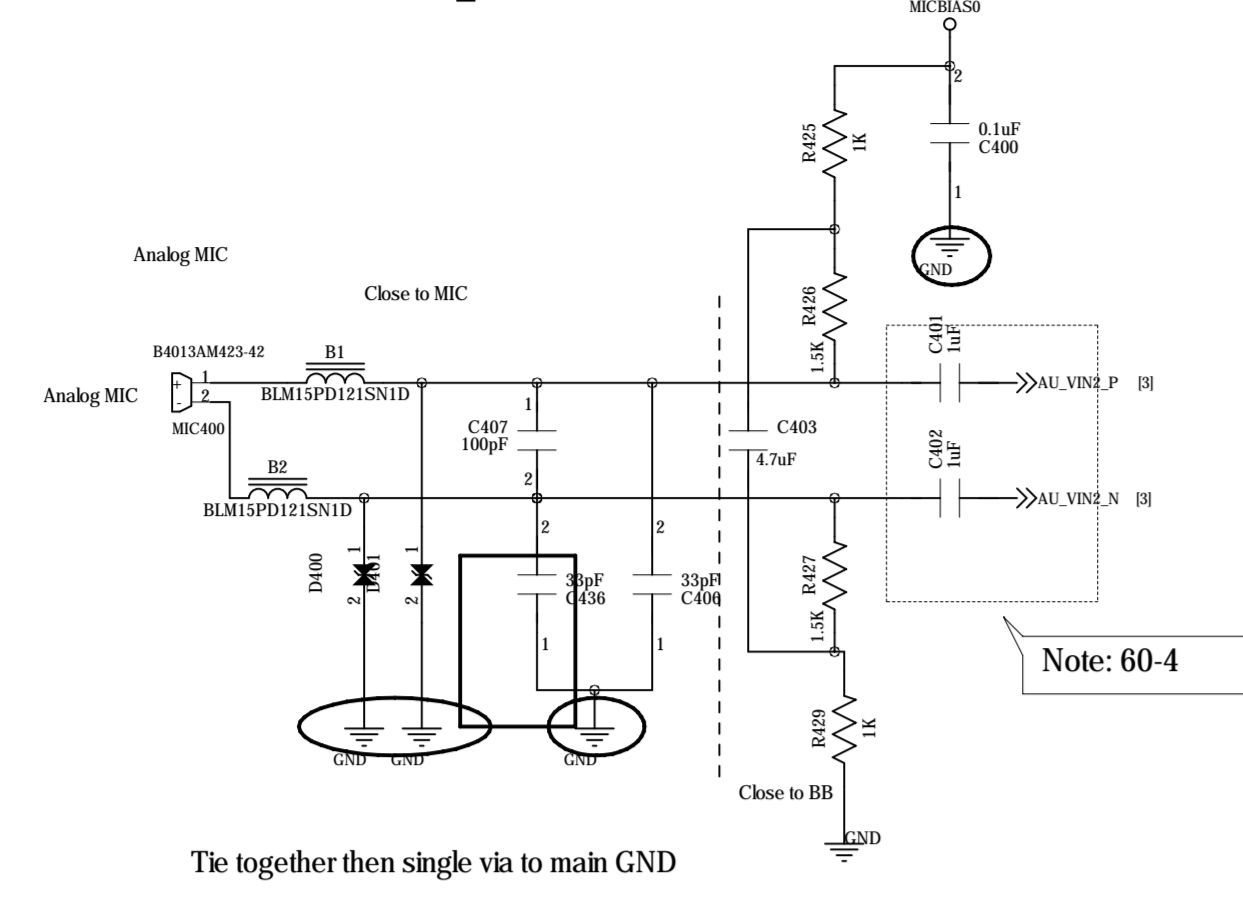
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CODE	SIZE	DRW/PC/NO	REV.

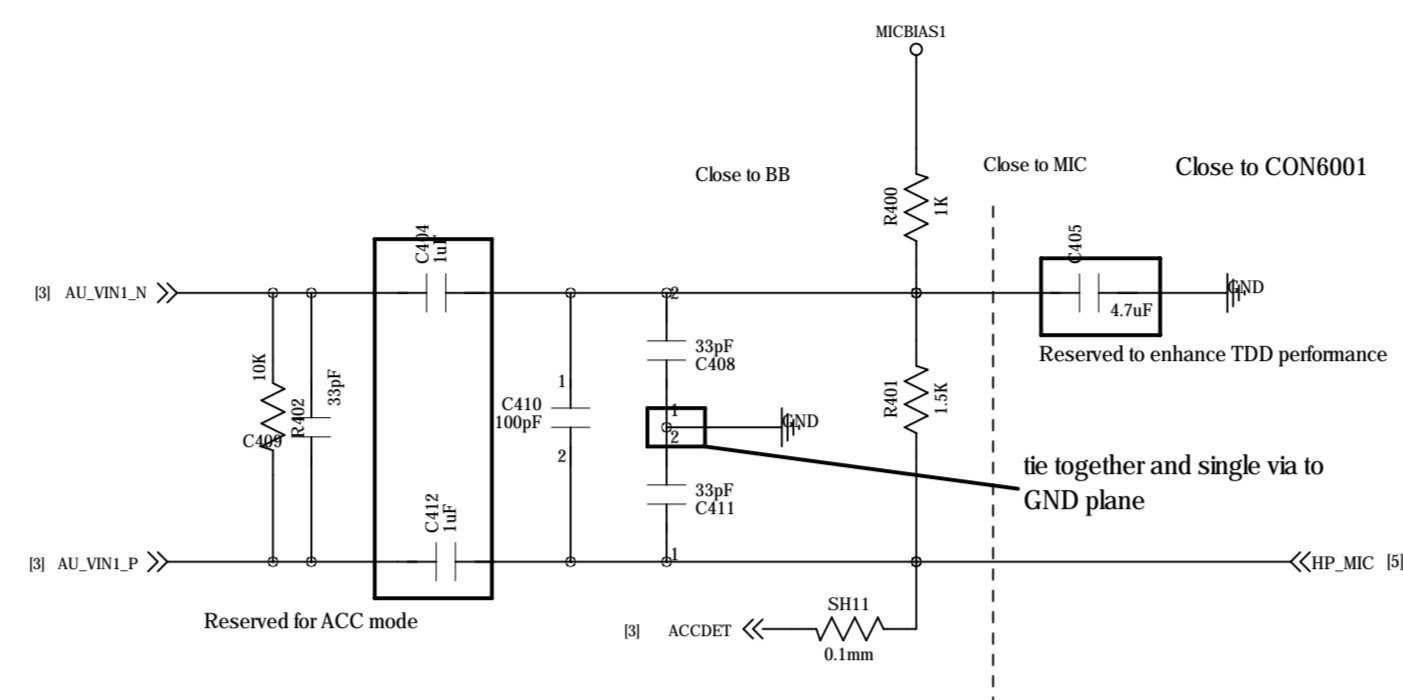
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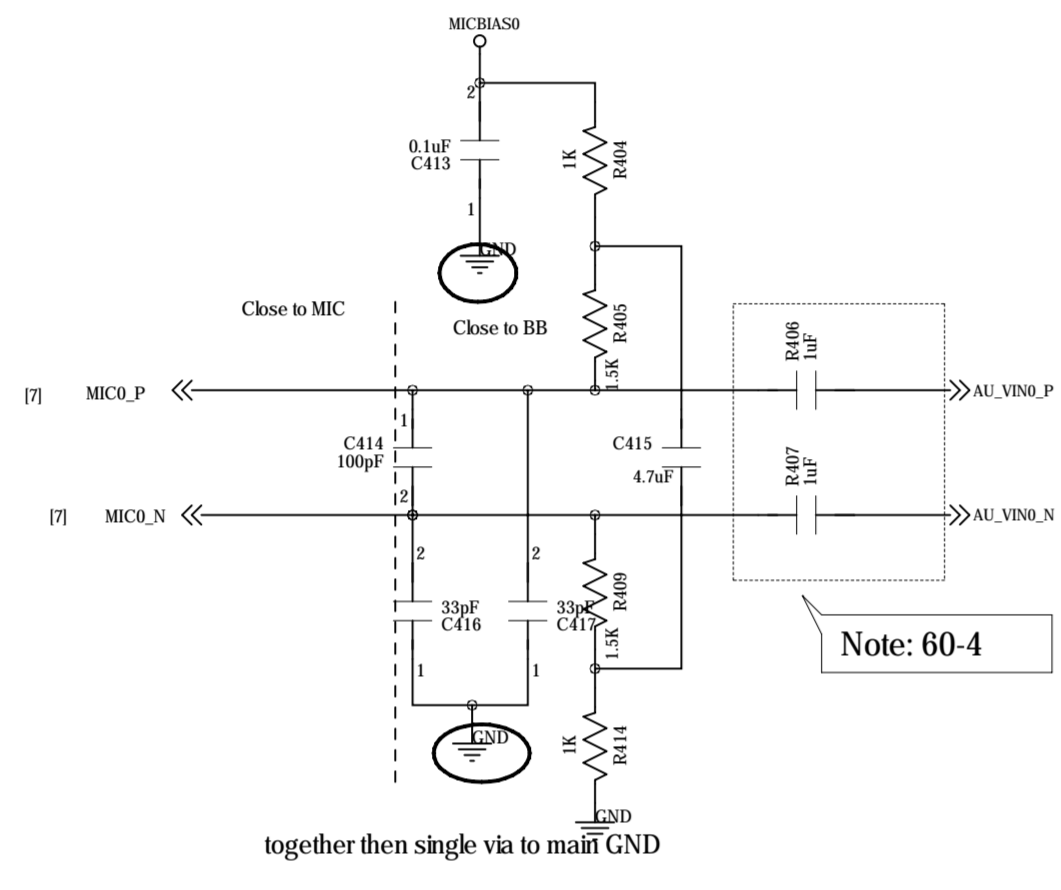
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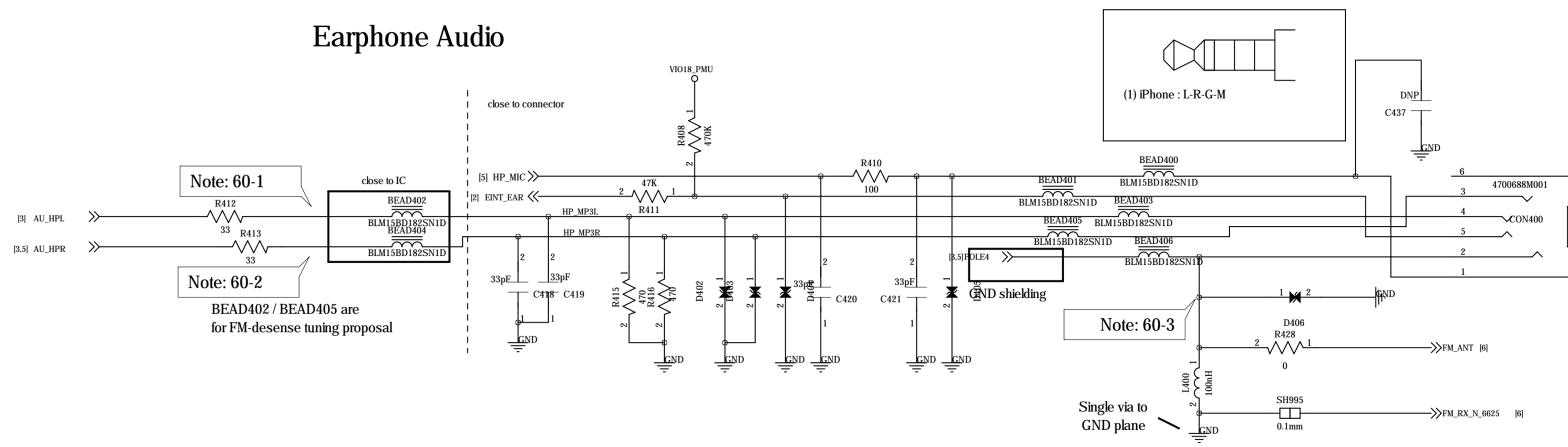
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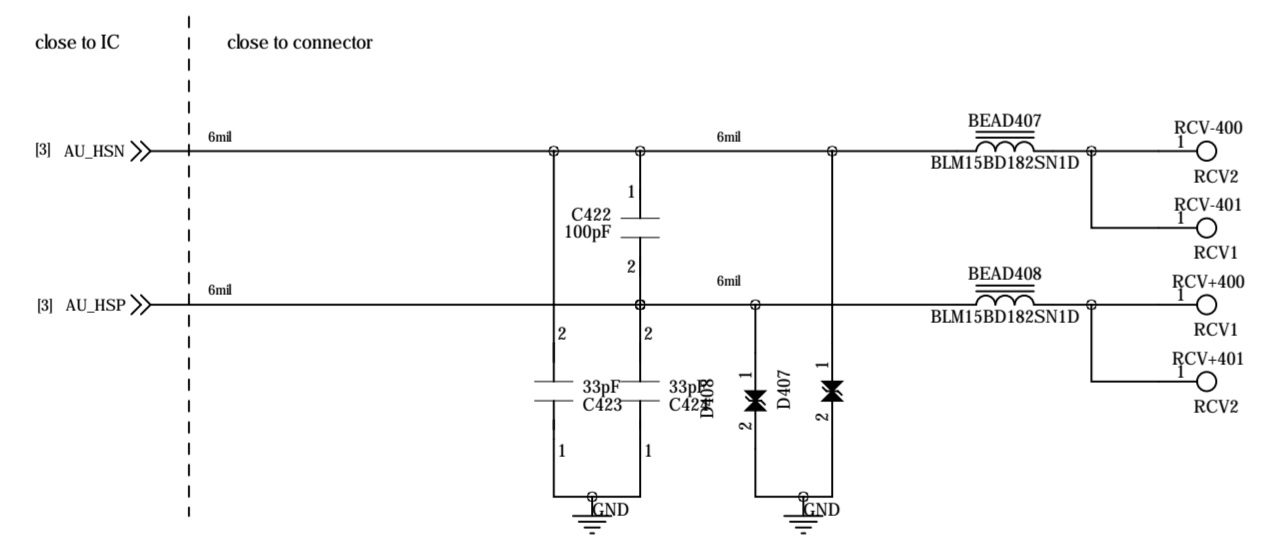
<Handset Microphone 1>



Earphone Audio

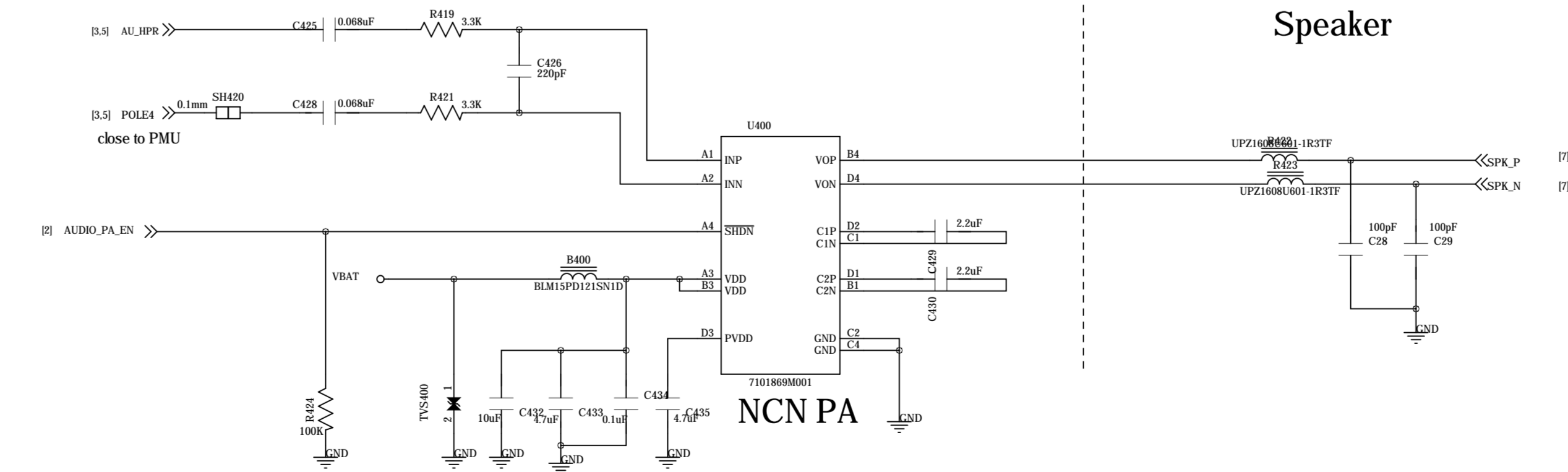


<Receiver>



<Audio PA>

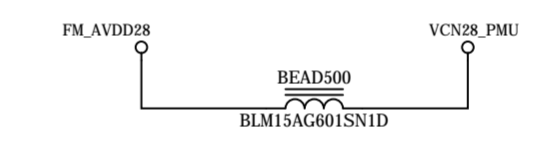
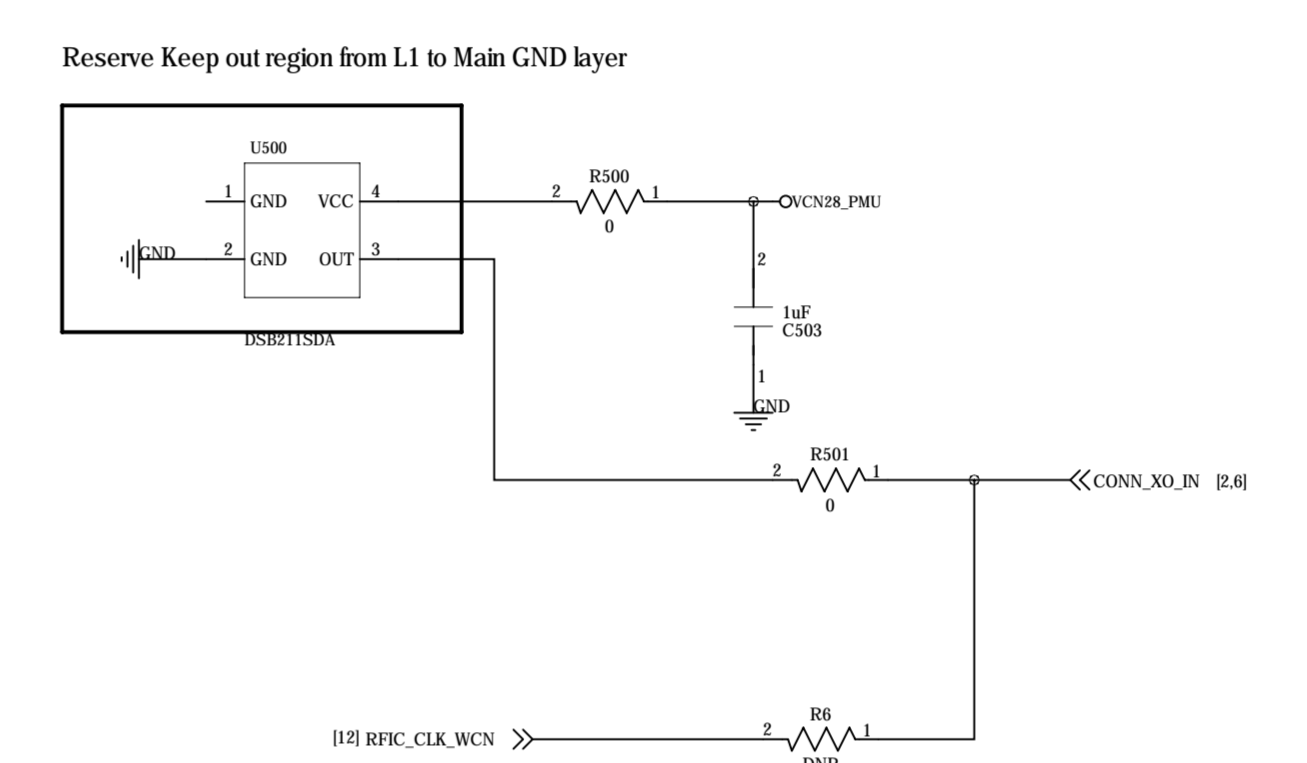
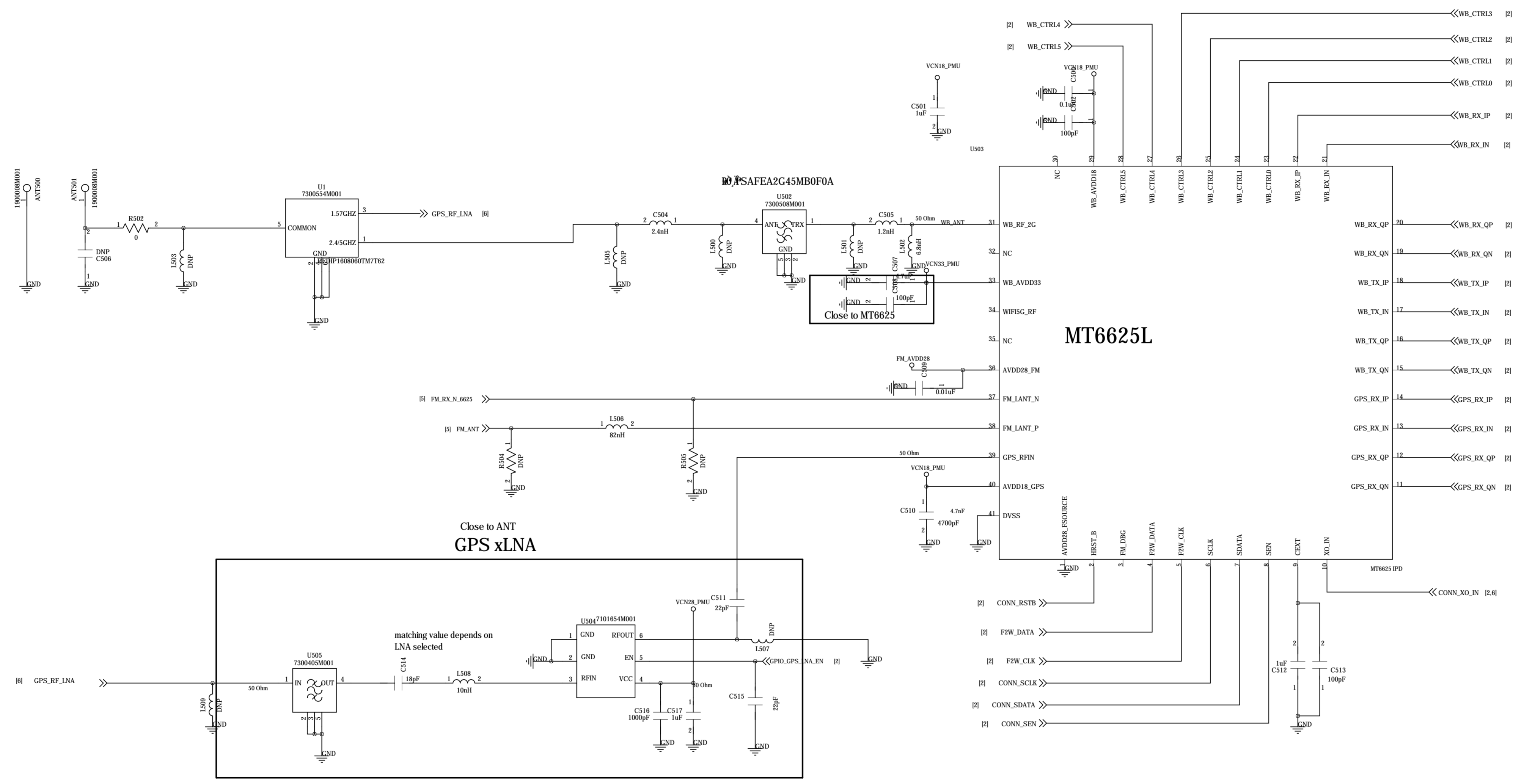
<Audio PA>



- Note 60-1: Part # of BEAD6002, BEAD6003, BEAD6004 and BEAD6005 needs changed to 'BLM18BD102SN1' for high THD performance (90dB) but this BOM change will result in FM RSSI 10dB degraded.
- Note 60-2: To reserve a resistor in HPL and HPR in series connection in order to optimize headphone pop noise. The recommended value of this resistor is 33R. If care Pop noise very much, need reserve analog switch. For the detail information, please refer to audio and speech design note or contact MTK support team. must surround shield with GND.
- Note 60-3: Layout trace from MT6355 ball J3 AUDREFN to Audio jack GND refer to audio and speech design note or contact MTK support team. must surround shield with GND.
- Note 60-4: 0.1uF uF for ACC mode (1uF for WB_AMR Speech/0.1uF for NB_AMR Speech) 0 ohm for DCC mode

COMPANY:		TITLE:	
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LP#	ECO#	APPROVED	DATE

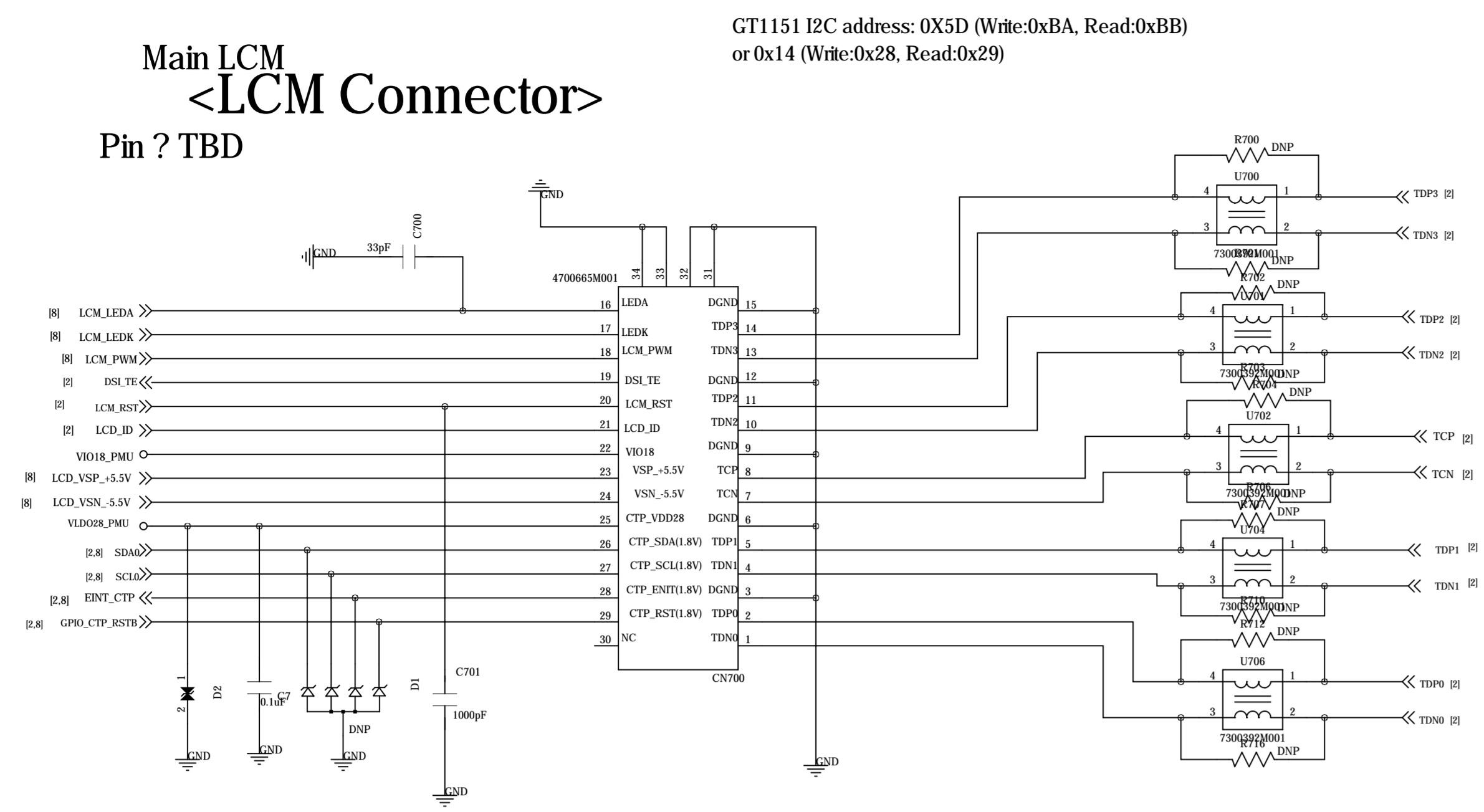


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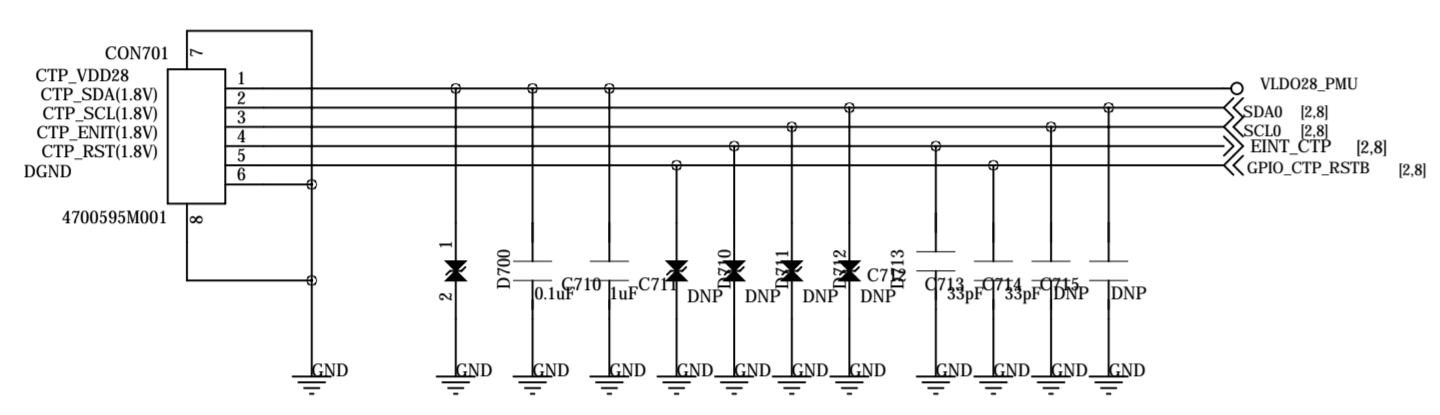
REVISION RECORD			
ITER	ECO NO.	APPROVED	DATE

Main LCM <LCM Connector>

Pin ? TBD

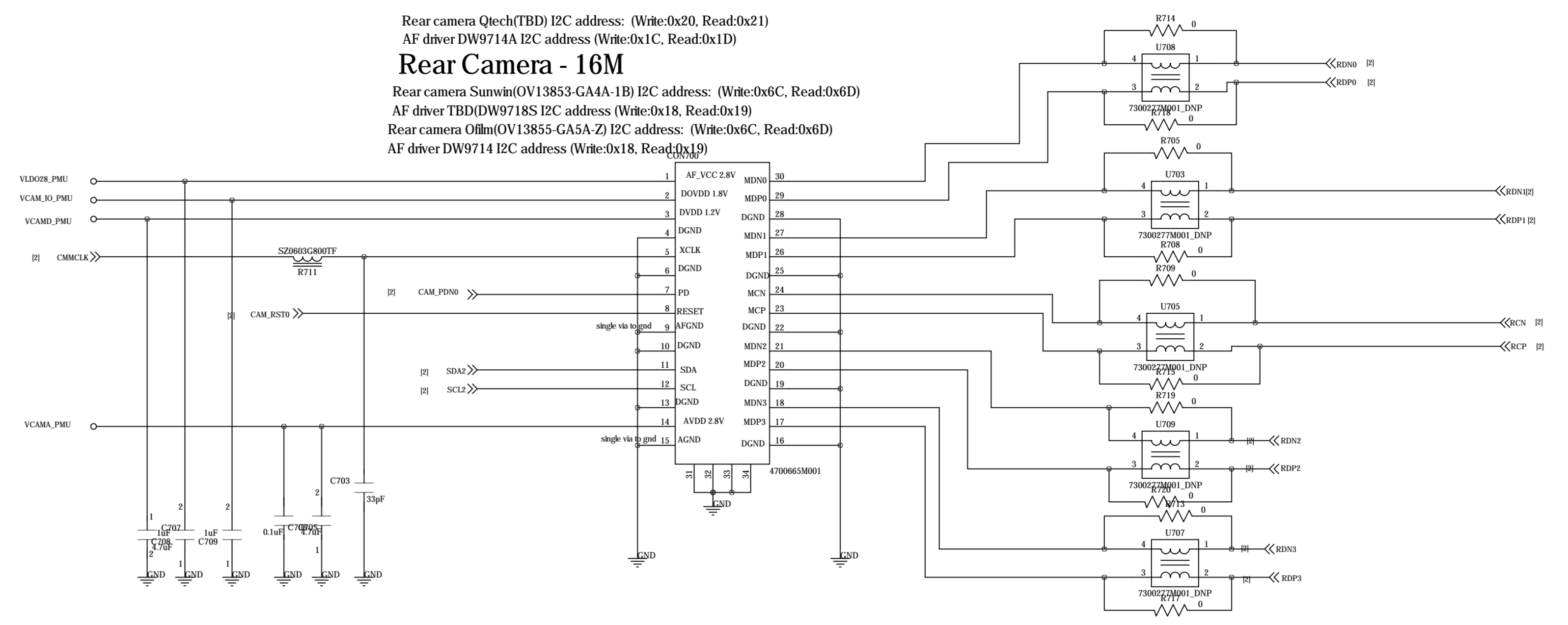


CTP

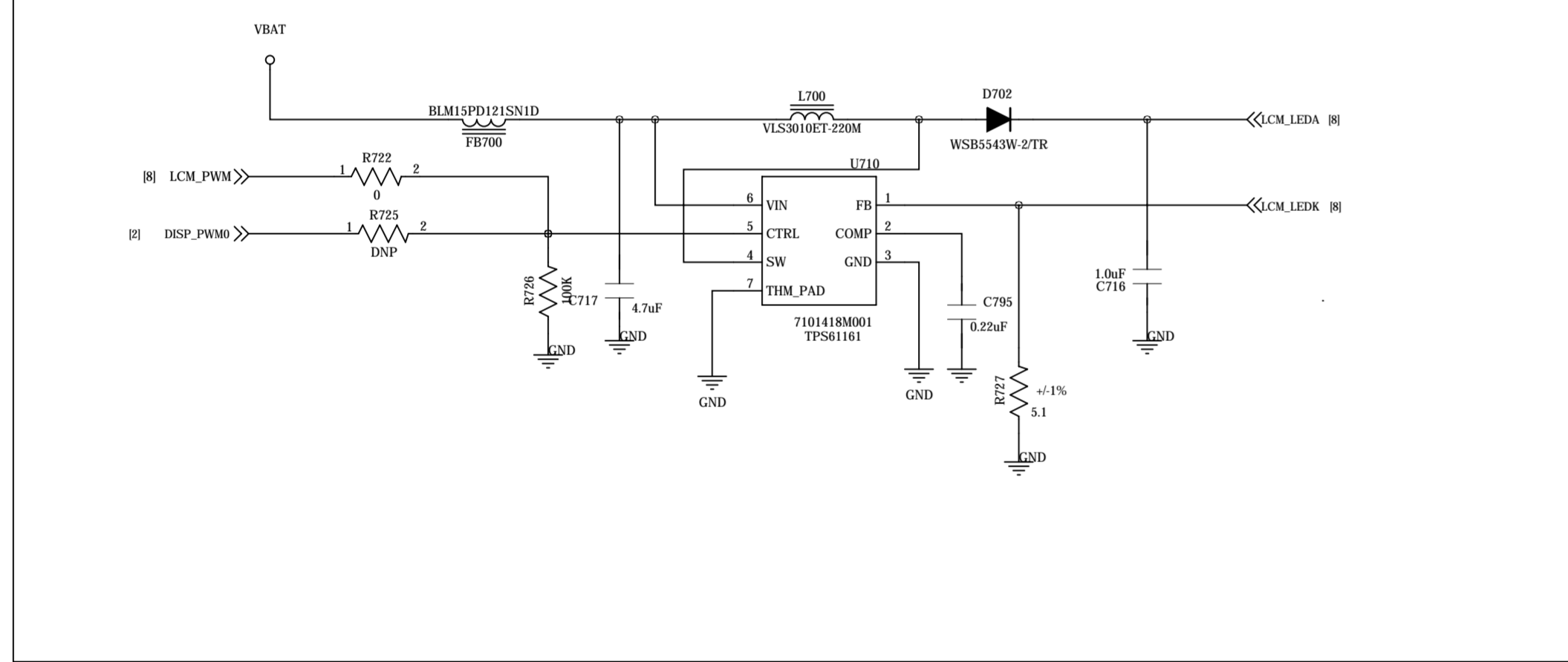


LCM ID setting				
1.8V	TCL	TXD	Supply2	Supply3
1.8V	R1=20K	R1=10K	R1=NC	R1=10K
1.8V	NC	R2=20K	R2=20K	R2=10K

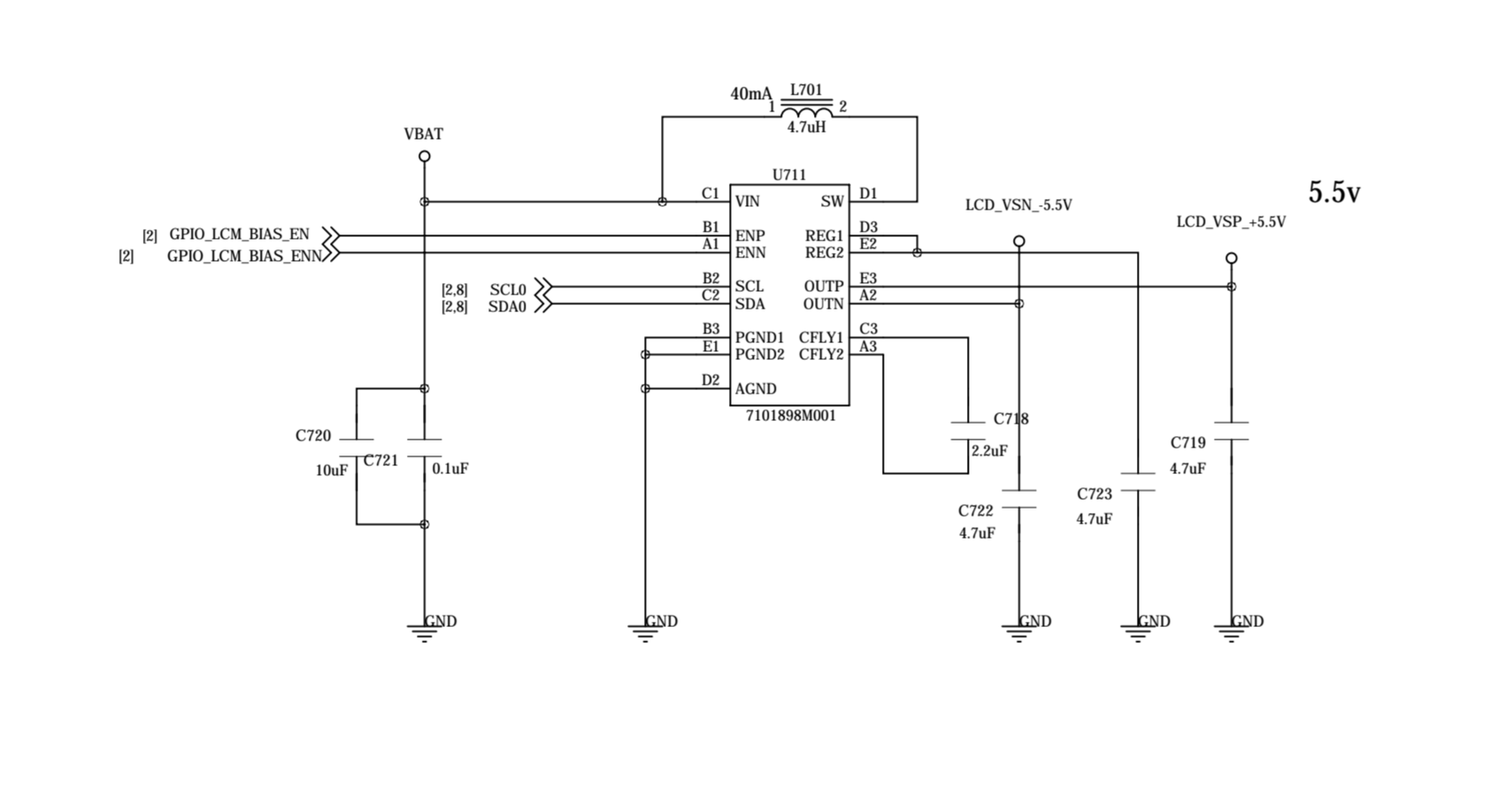
<Rear Camera Connector>



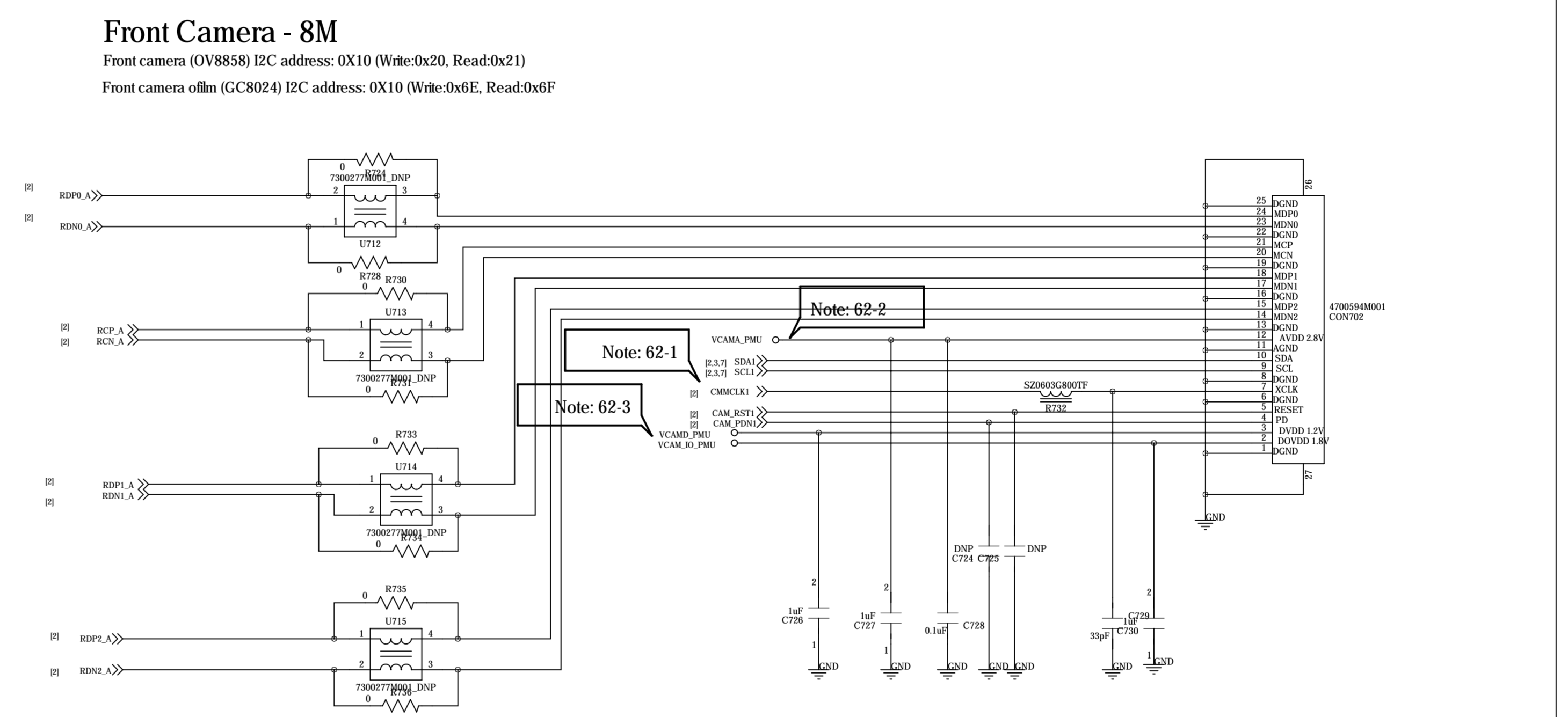
<LCM Backlight LED Driver>



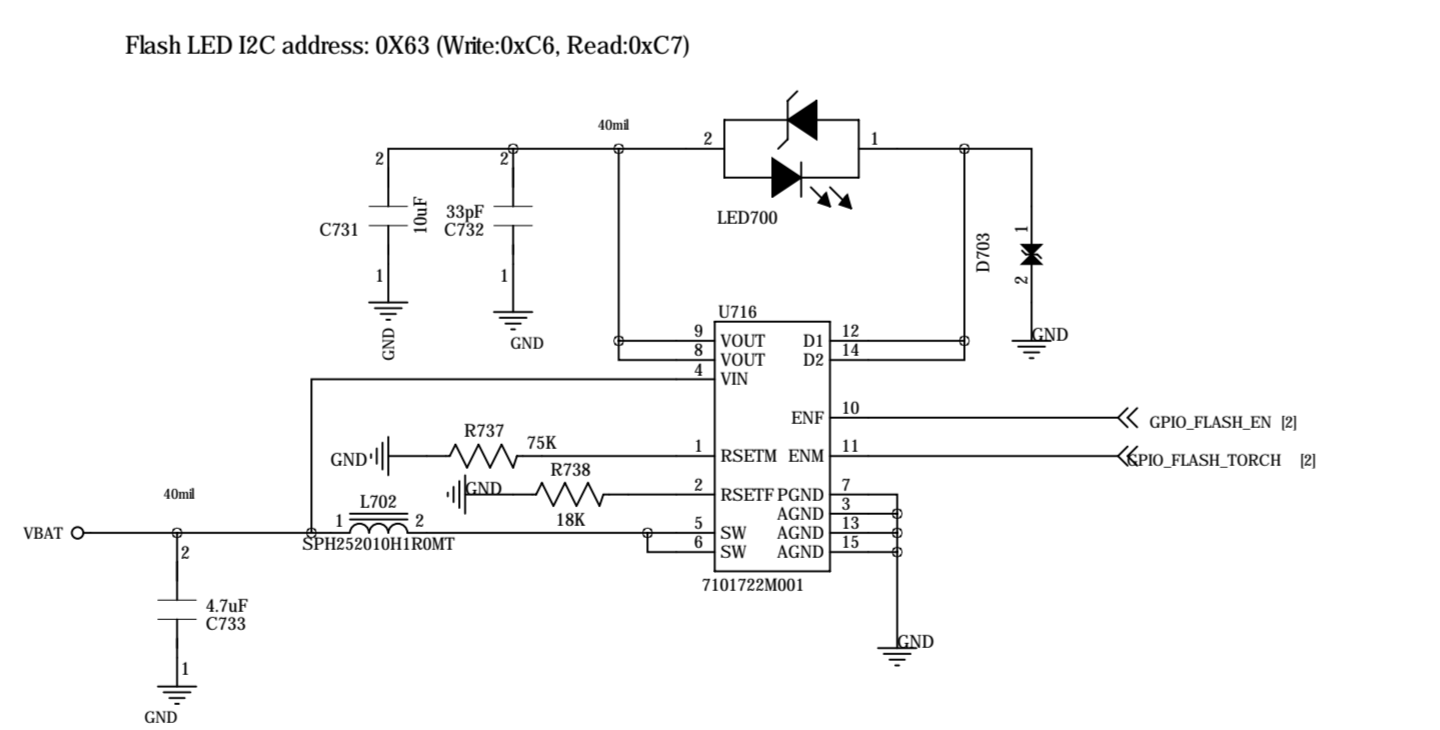
<LCM analog power>



<Front Camera Connector>



<Flash LED 5V Boost>

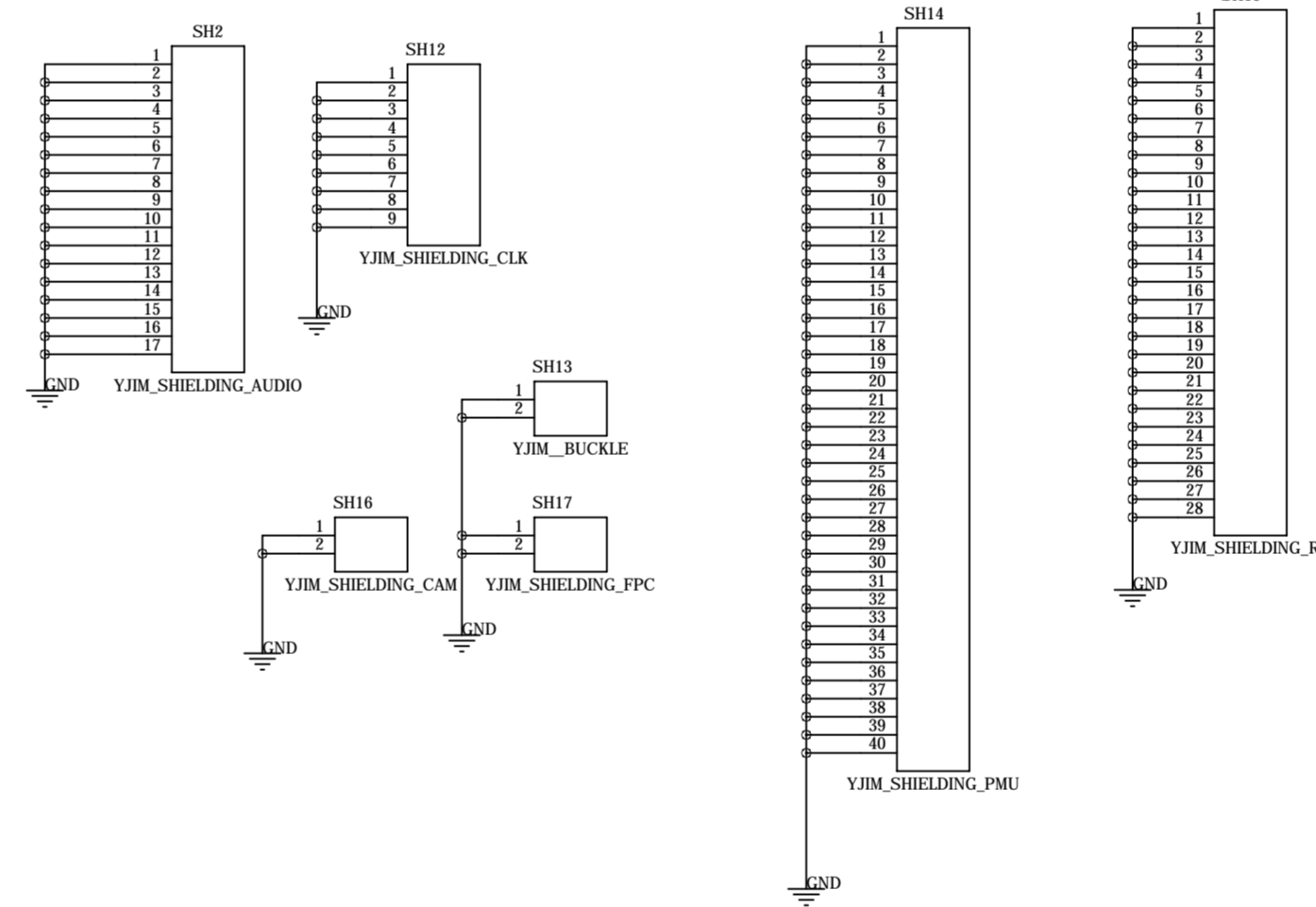
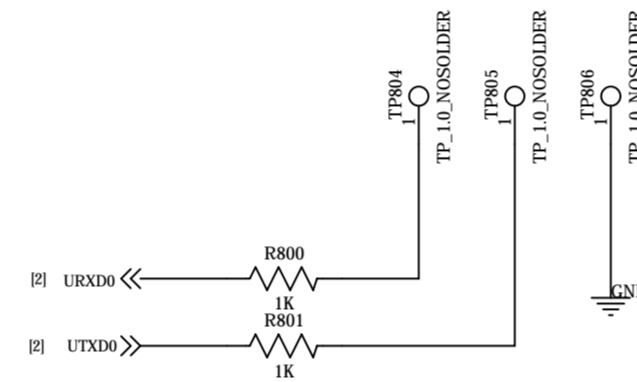
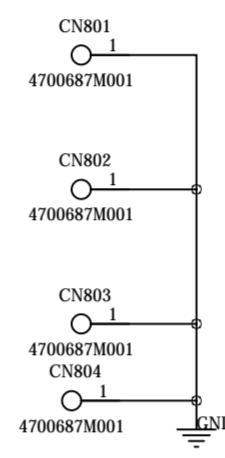
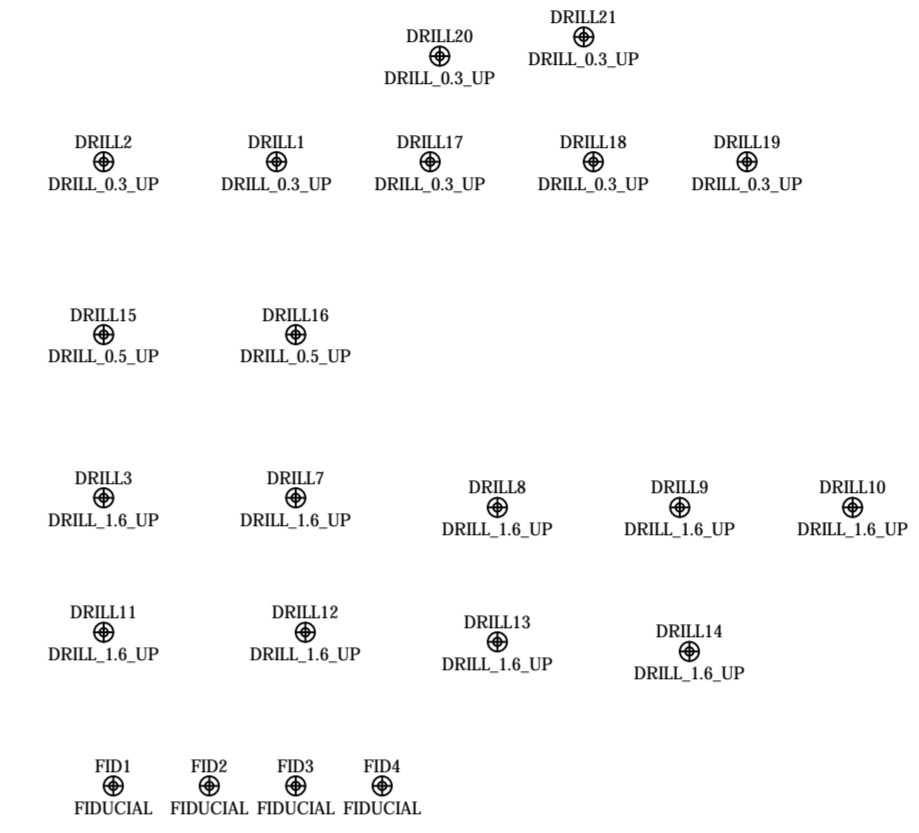
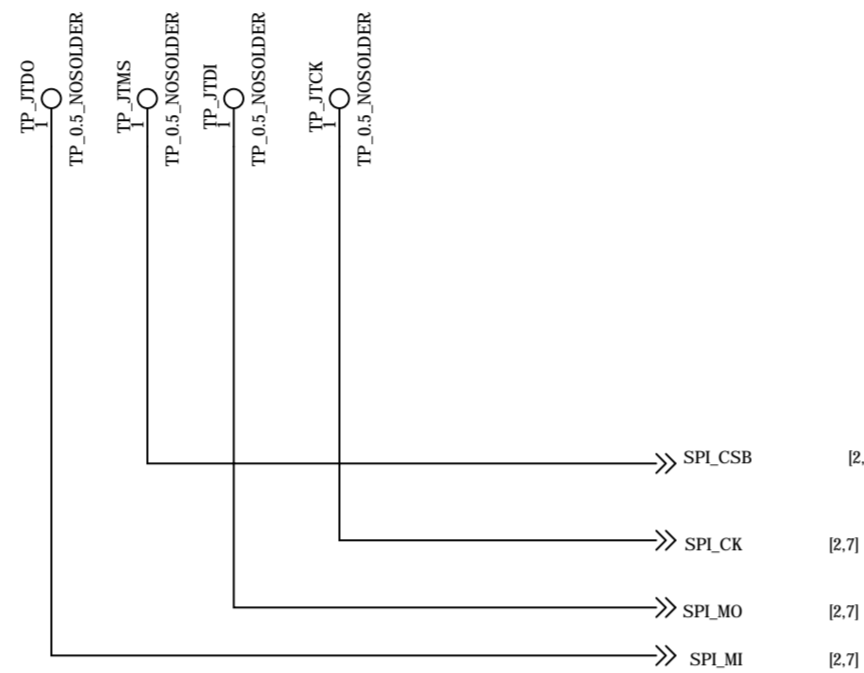


- Note 62-1: The VCC of I2C_1/2 is pulled to "VIO18_PWD".
- Note 62-2: Reserved LDO For SUB CAM PIP FUNCTION (VCAMA)
- Note 62-3: Reserved LDO For SUB CAM PIP FUNCTION (VCAMD)

COMPANY:			
TITLE:			
DRAWN:	DATED:	CODE:	SIZE:
CHECKED:	DATED:	DRAWING NO.	REV.
QUALITY CONTROL:	DATED:	SCALE:	
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REVISION RECORD			
LT#	ECO NO.	APPROVED	DATE

Note 12-1: If JTAG is set to N/A by trapping pin. Do not set GPIO[95:98] as JTAG mode (Aux Func. 7) in DCT tool (dws file).

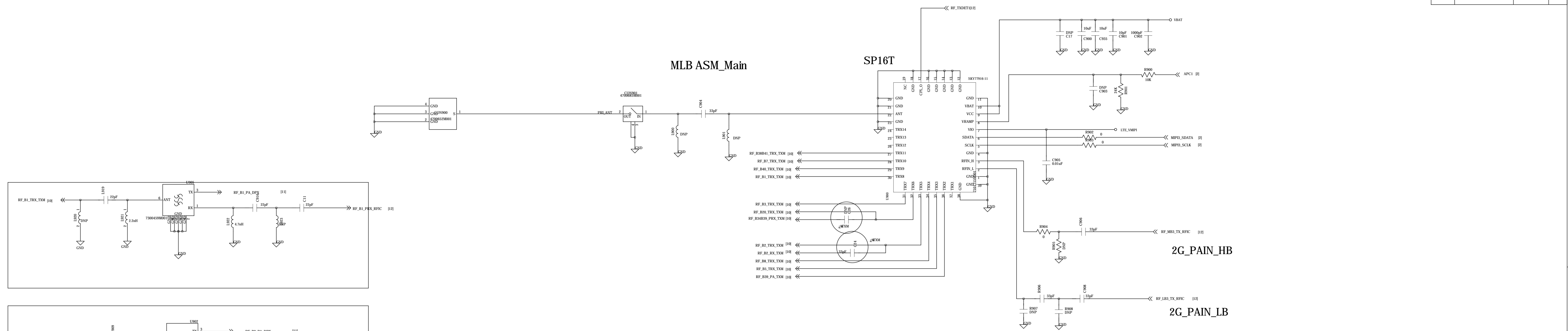


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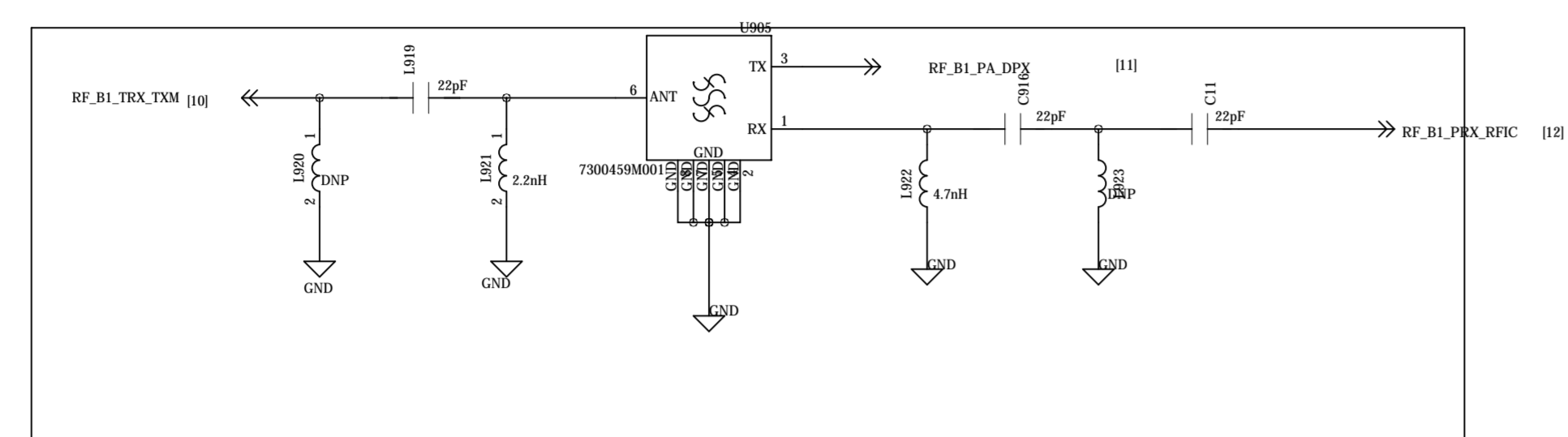
COMPANY:

TITLE:

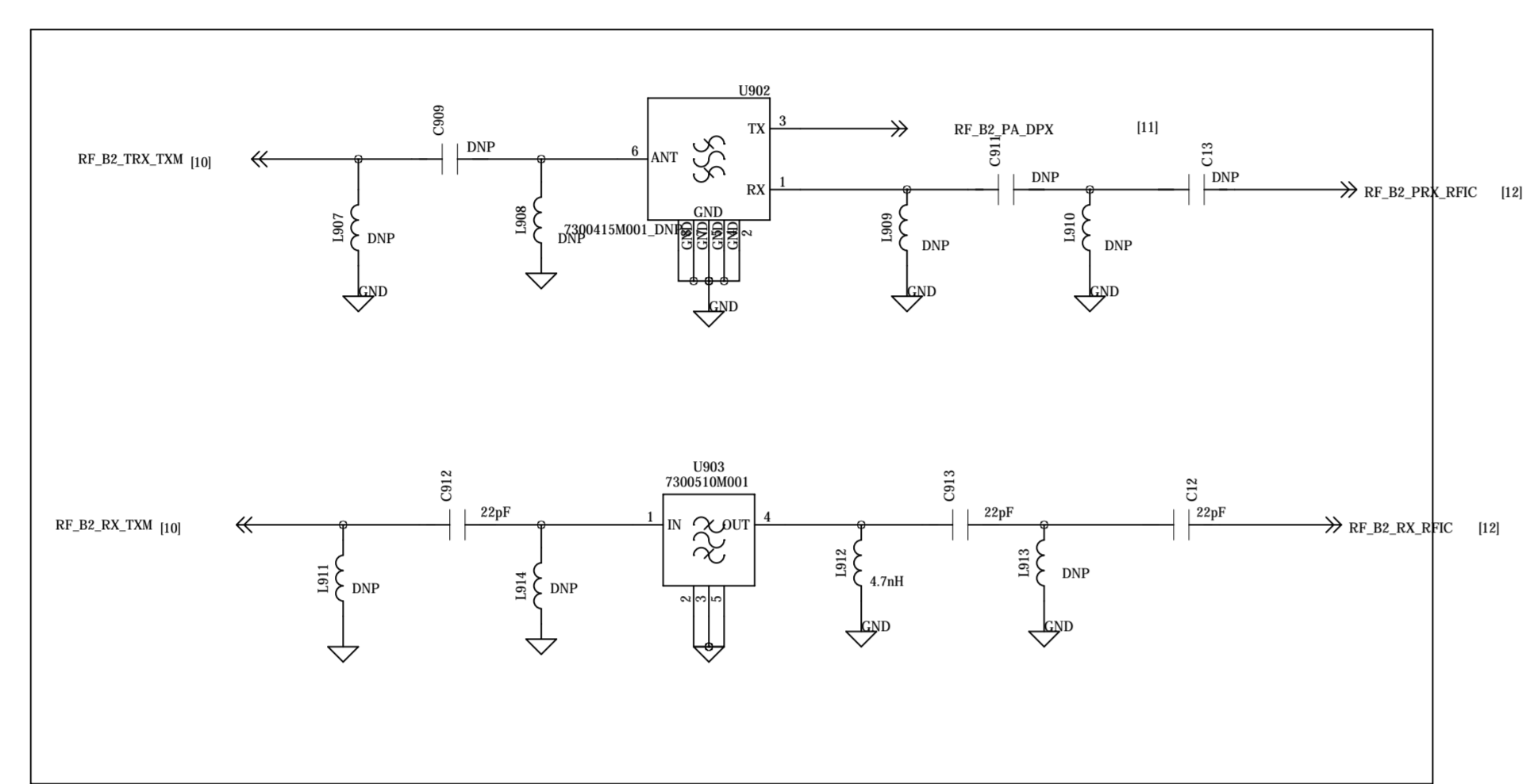
REVISION RECORD			
LTB	ECO NO.	APPROVED	DATE



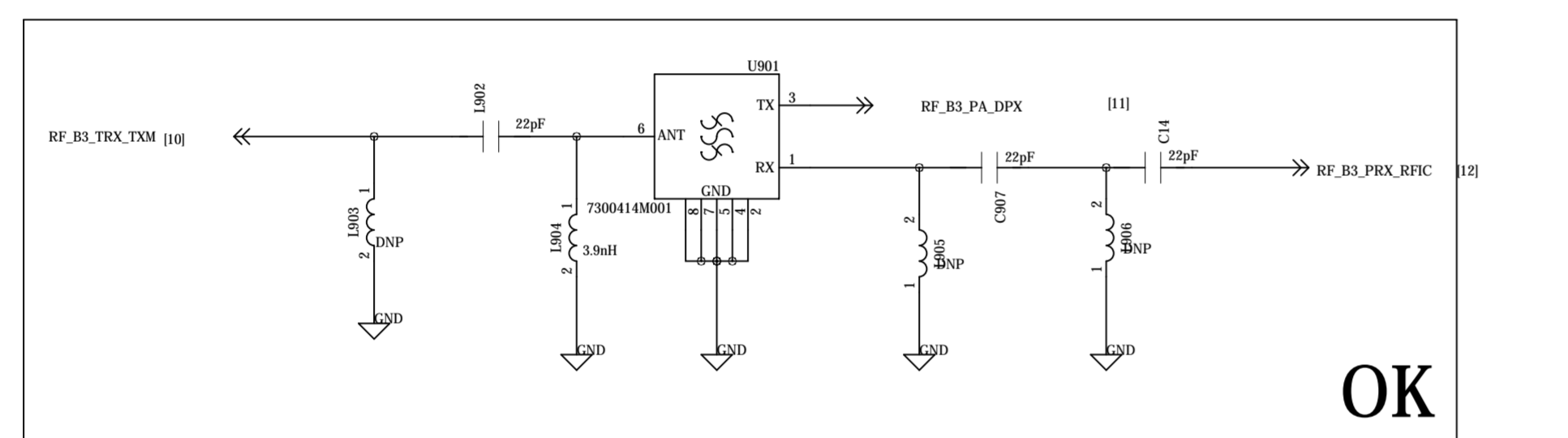
BAND1



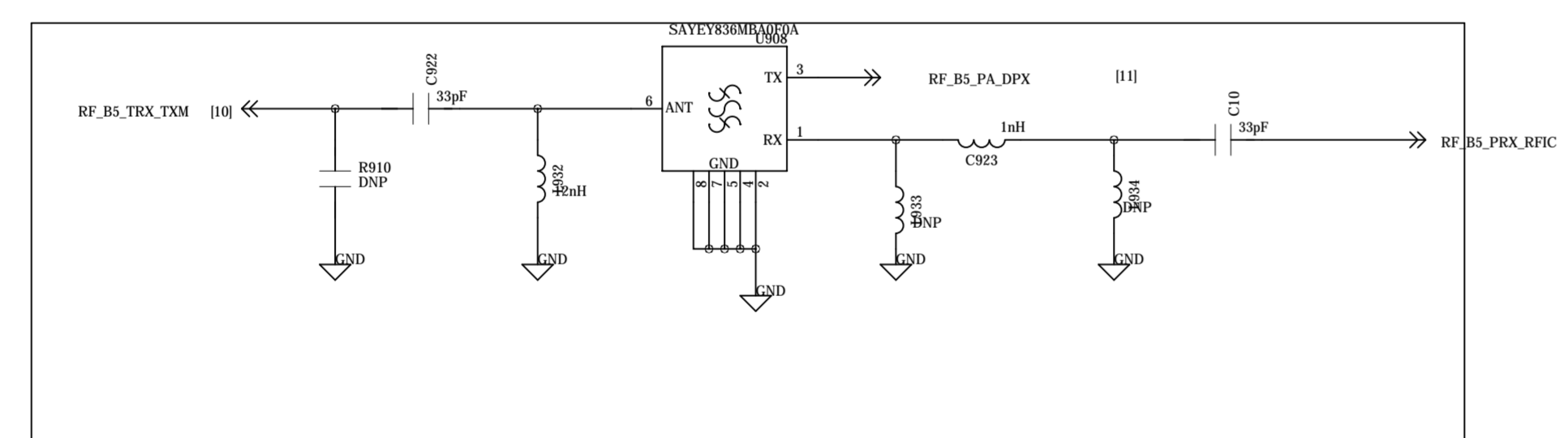
BAND2



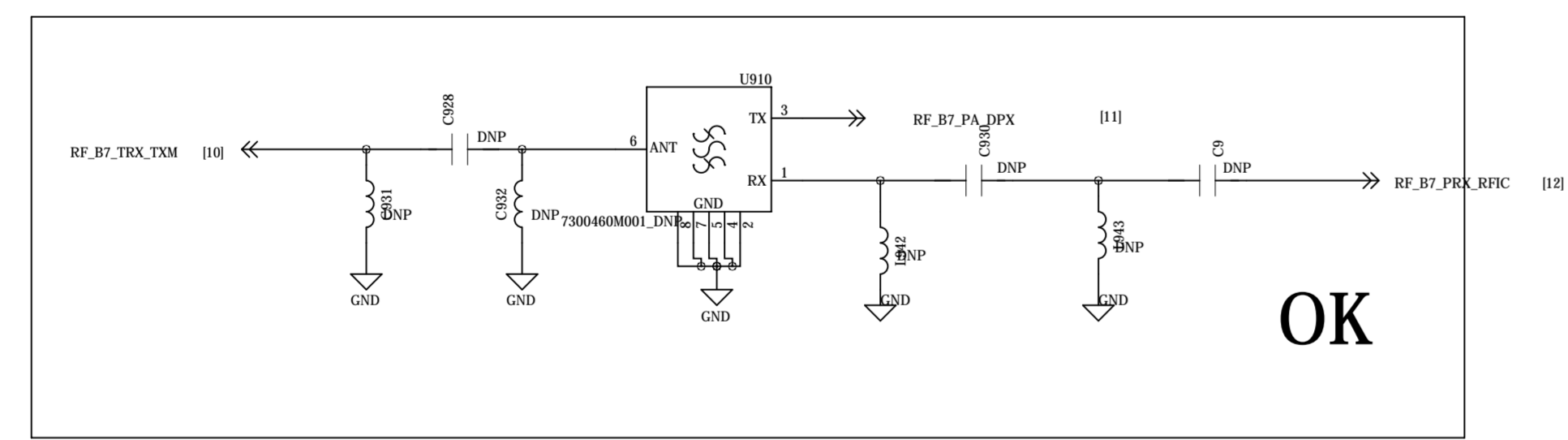
BAND3



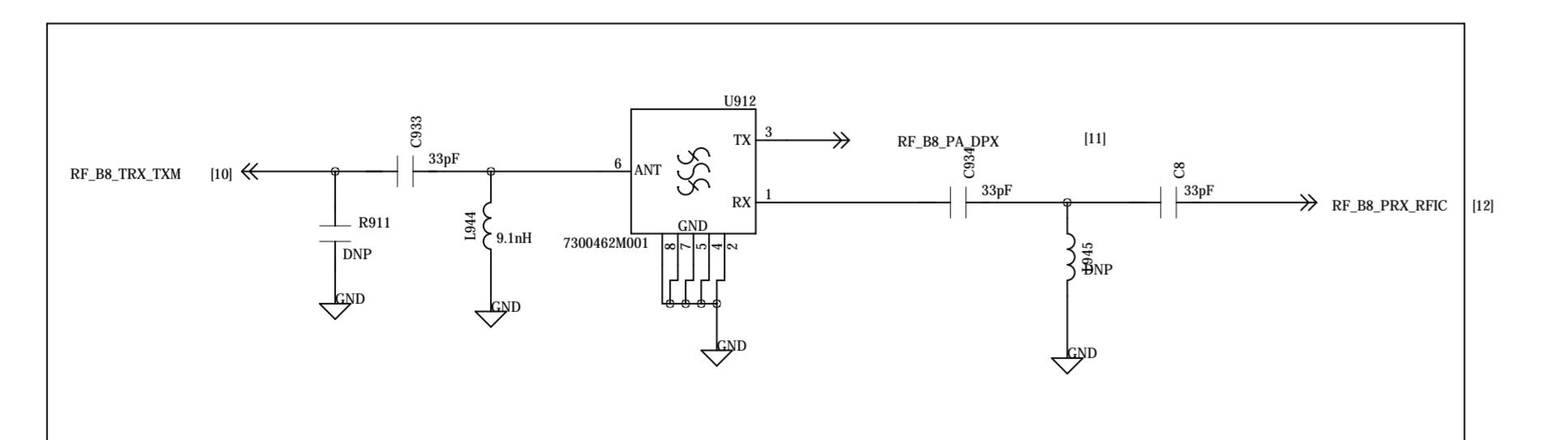
BAND5



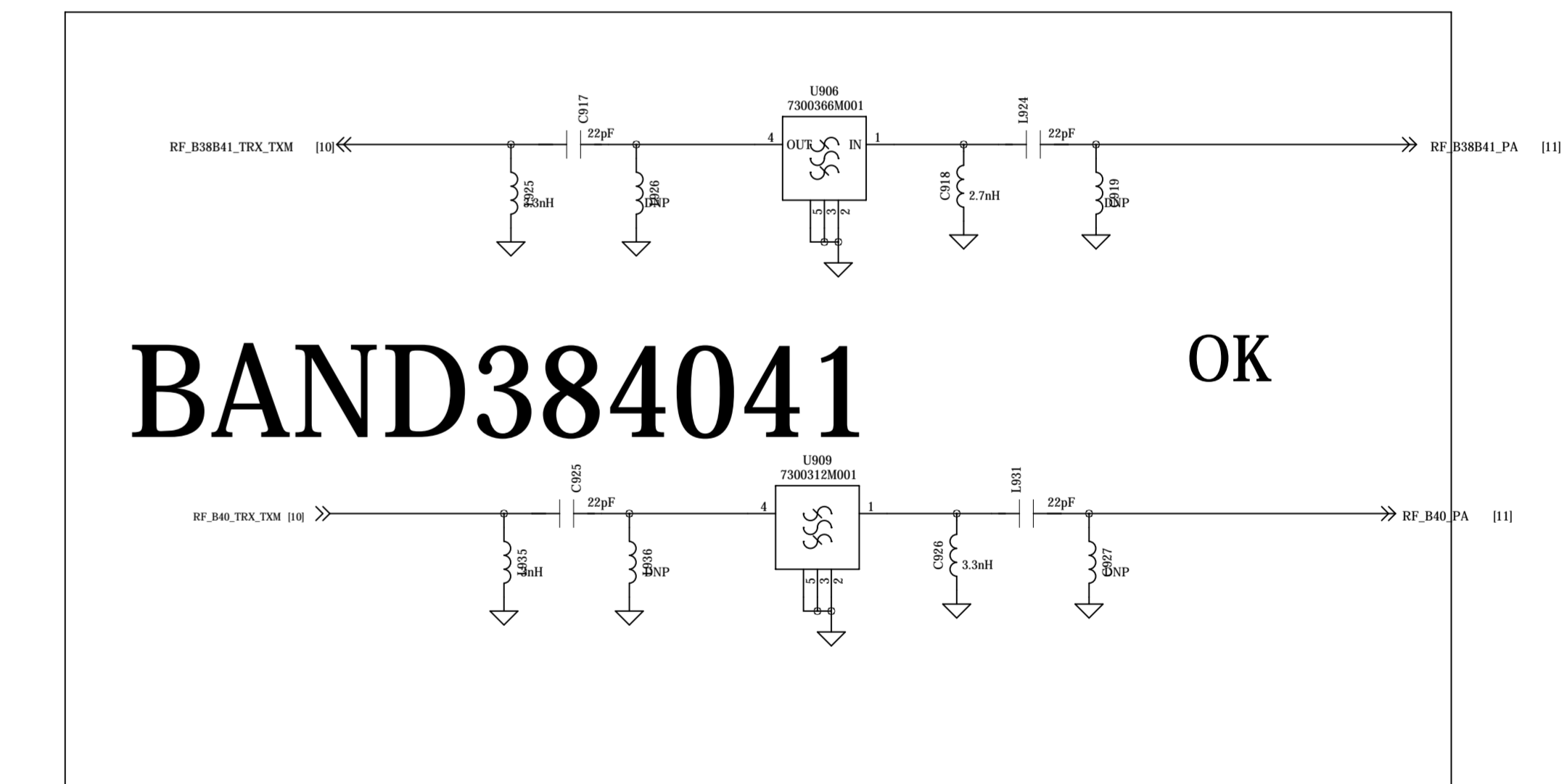
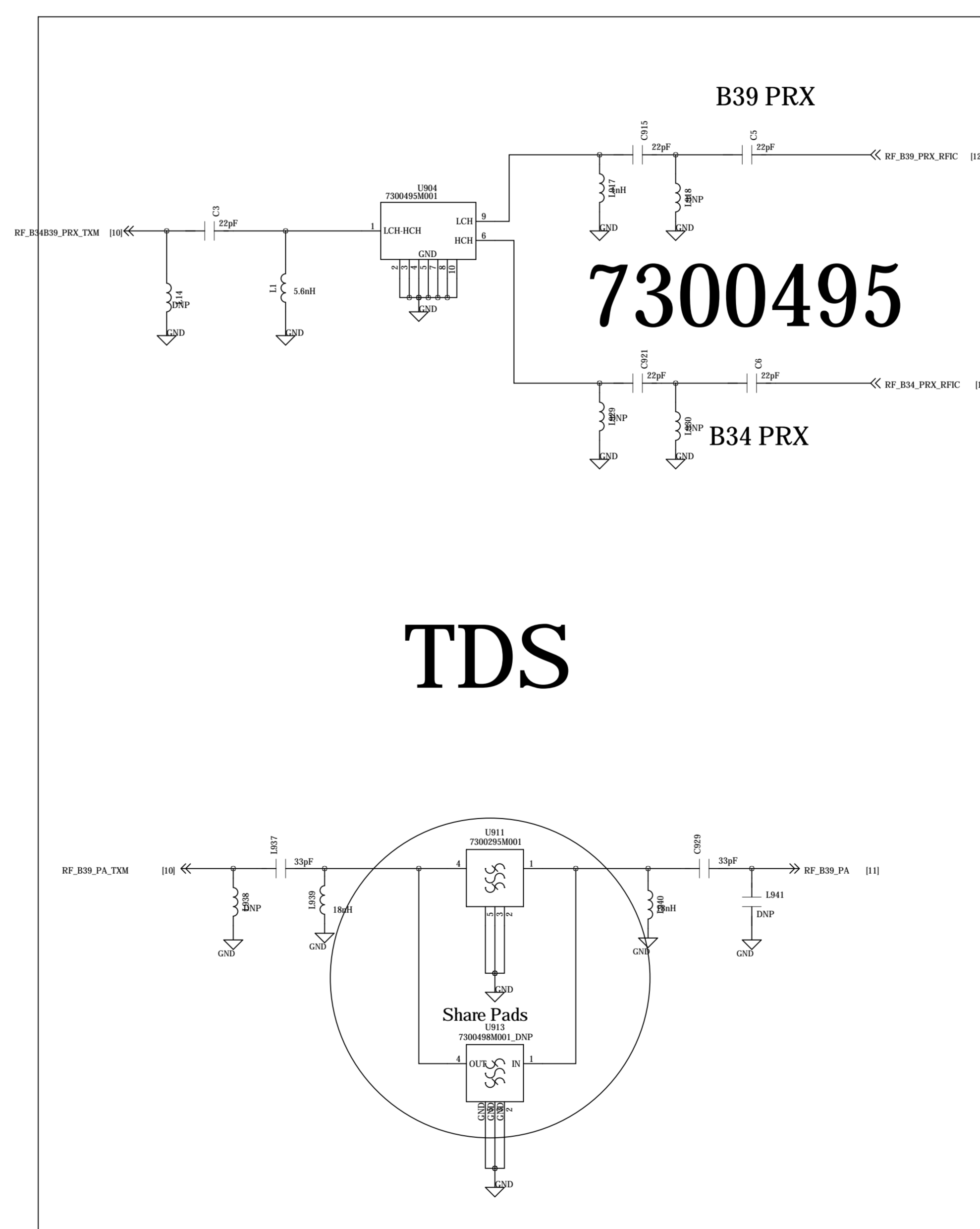
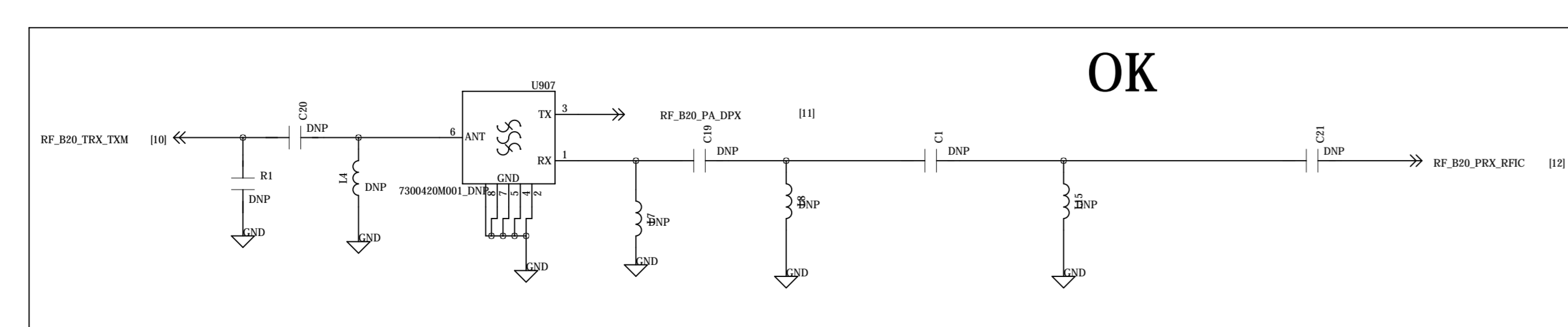
BAND7



BAND8

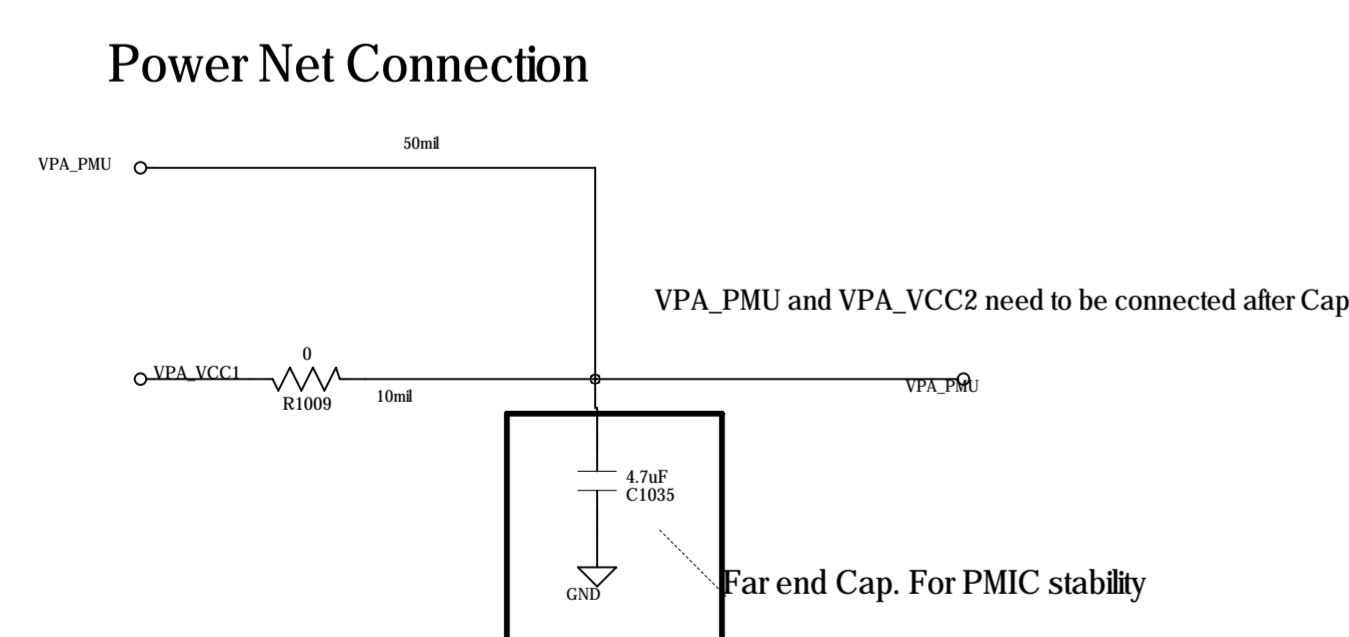
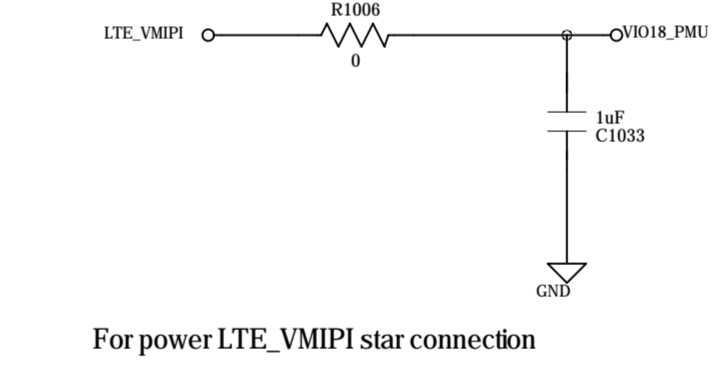
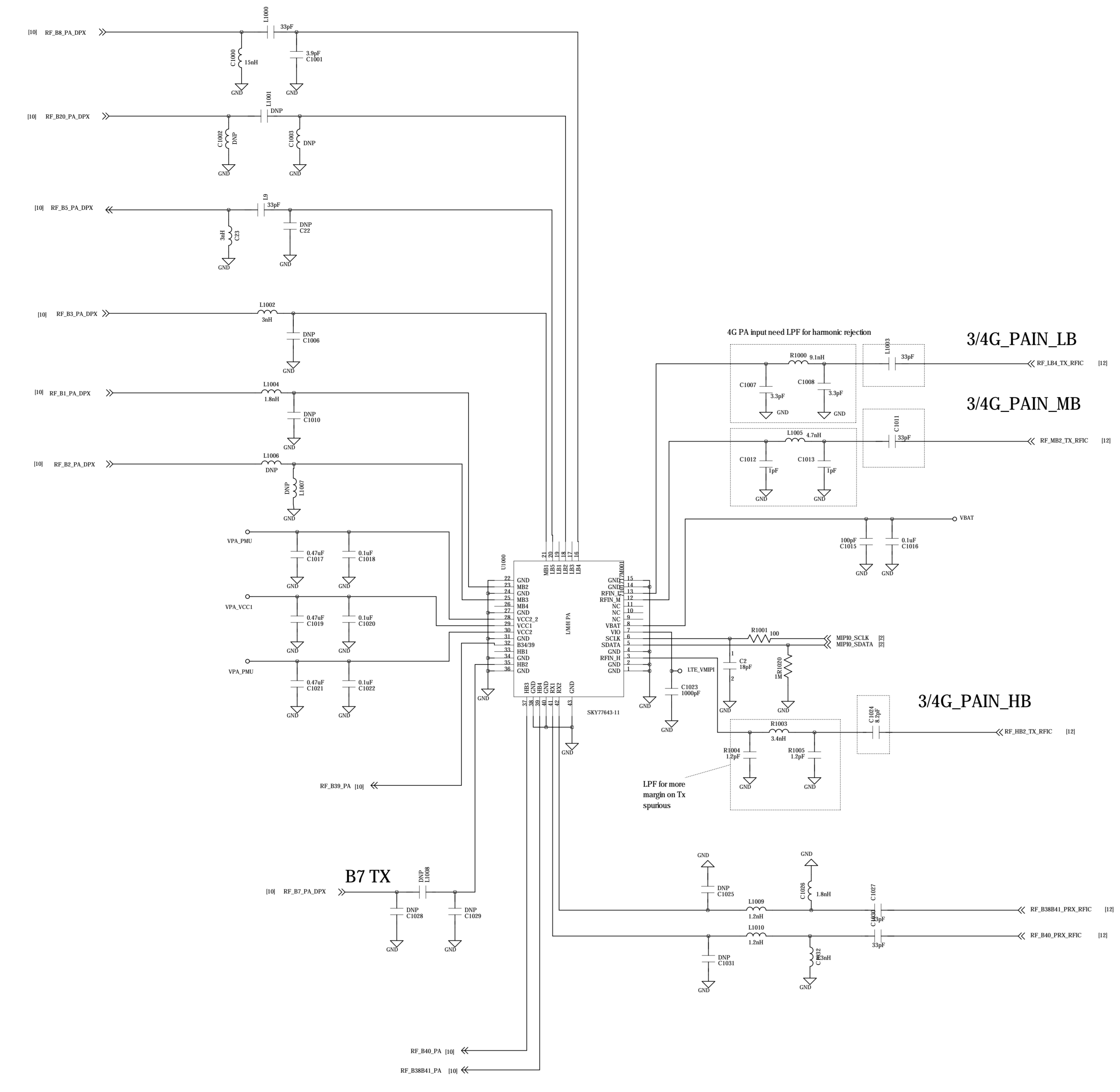


BAND20



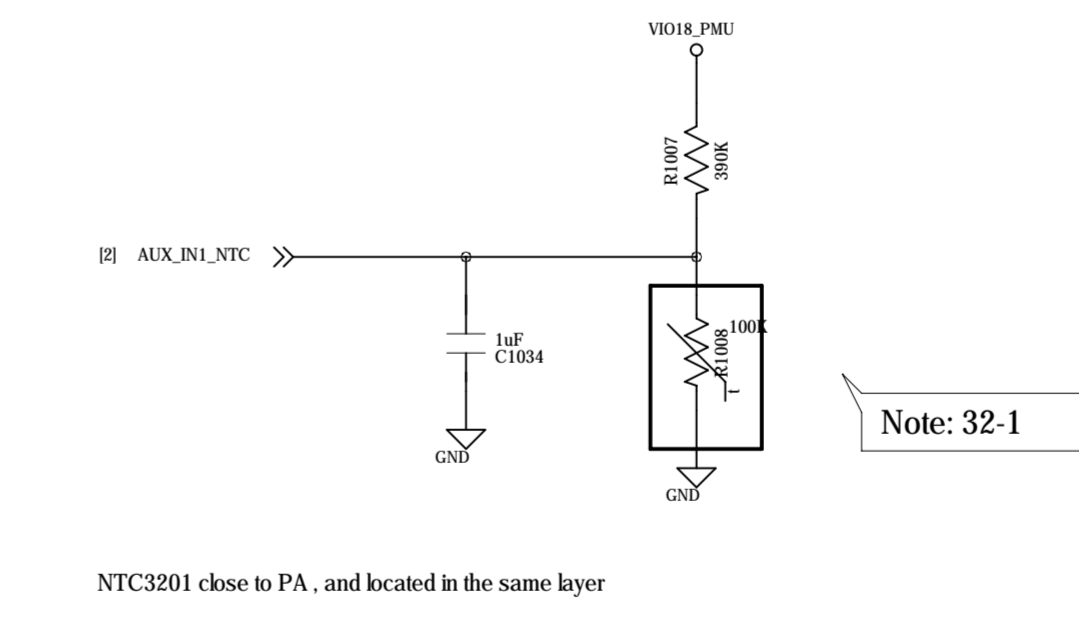
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CHECKED		DATED		SCALE		SHEET		OF			
QUALITY CONTROL		DATED									
RELEASED		DATED									

REVISION RECORD			
LT#	ECO NO.	APPROVED	DATE



Note: B39/B41 dip-SAW can support both non-CA and B39/41 CA, the CA feature depends on CA modem development done.

Thermistor / To sense board level temperature



Schematic design notice of "32_RF_MT6176_RF_TX" page.
 Note 32-1: Reserved and will be removed

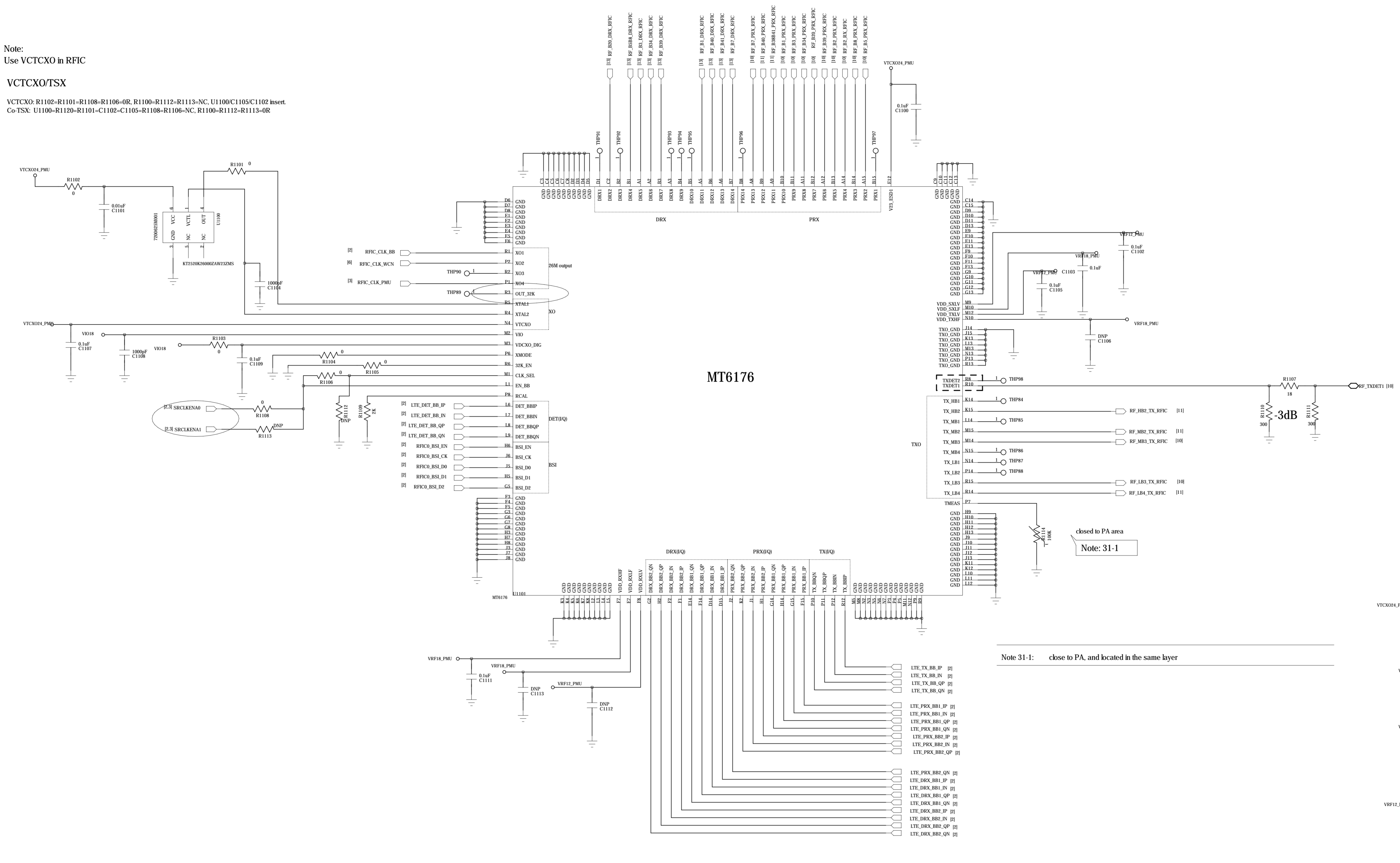
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TITLE:					
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CHECKED:	DATE:				
QUALITY CONTROL:	DATE:	SCALE:			SHEET OF
RELEASED:	DATE:				

REVISION RECORD			
ITR	ECO NO	APPROVED	DATE

Note:
Use VCTCXO in RFIC

VCTCXO/TSX

VCTCXO: R1102-R1101-R1108-R1106-OR, R1100-R1112-R1113-NC, U1100C1105C1102 Reset
Co-TSX: U1100-R1120-R1101-C1102-C1105-R1108-R1106-NC, R1100-R1112-R1113-OR

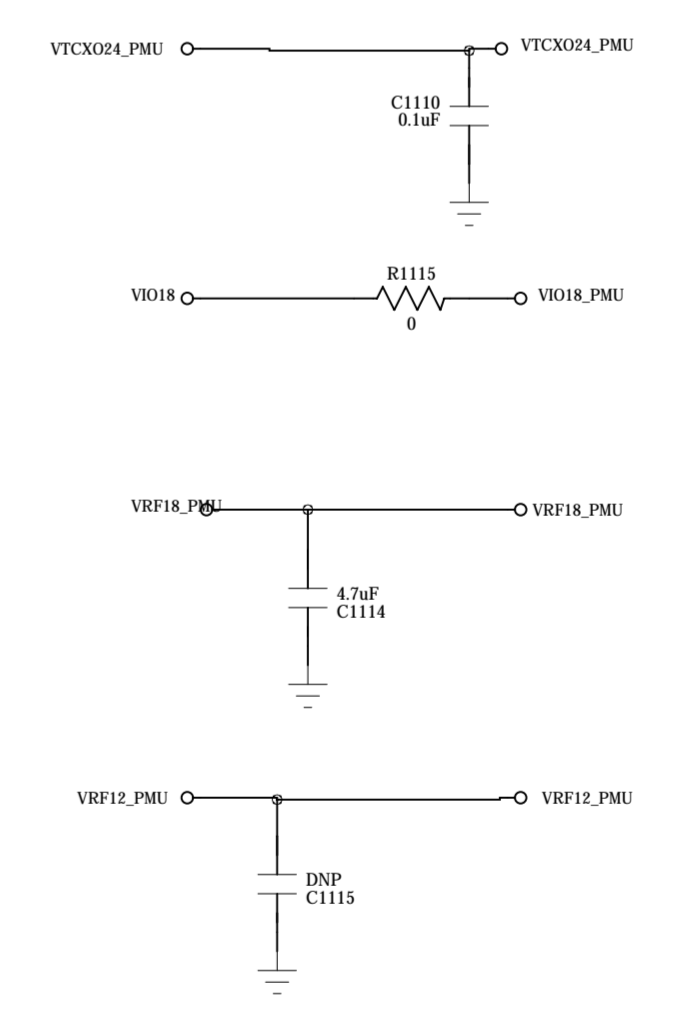


MT6176

Note: 31-1

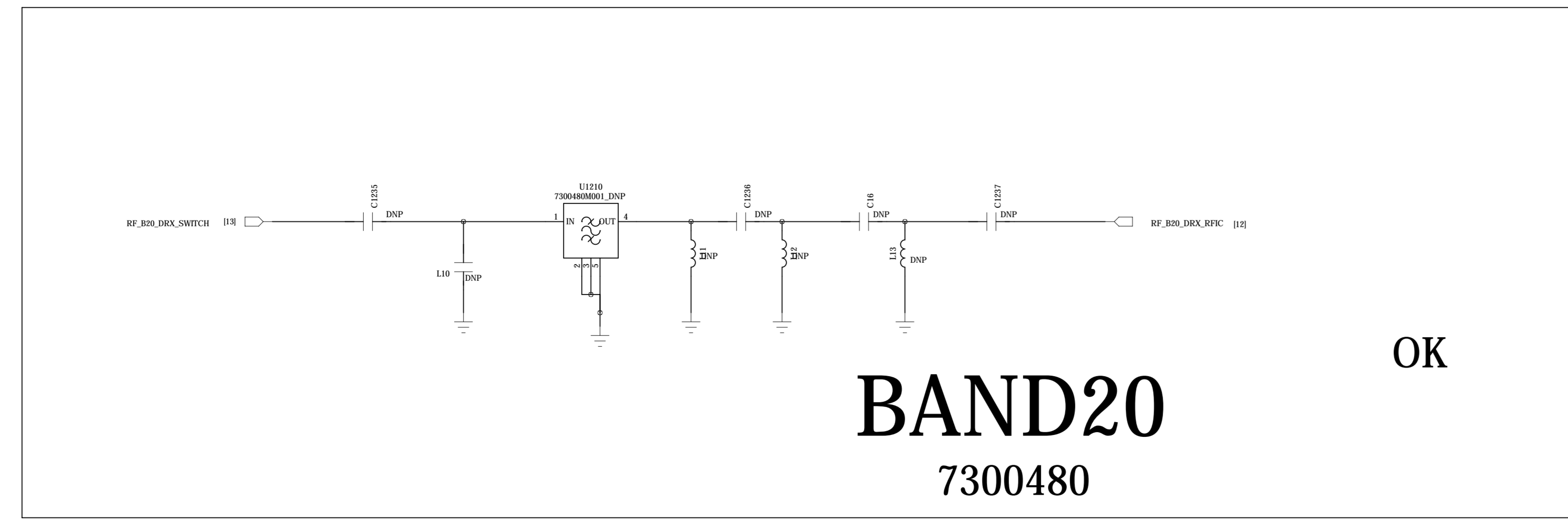
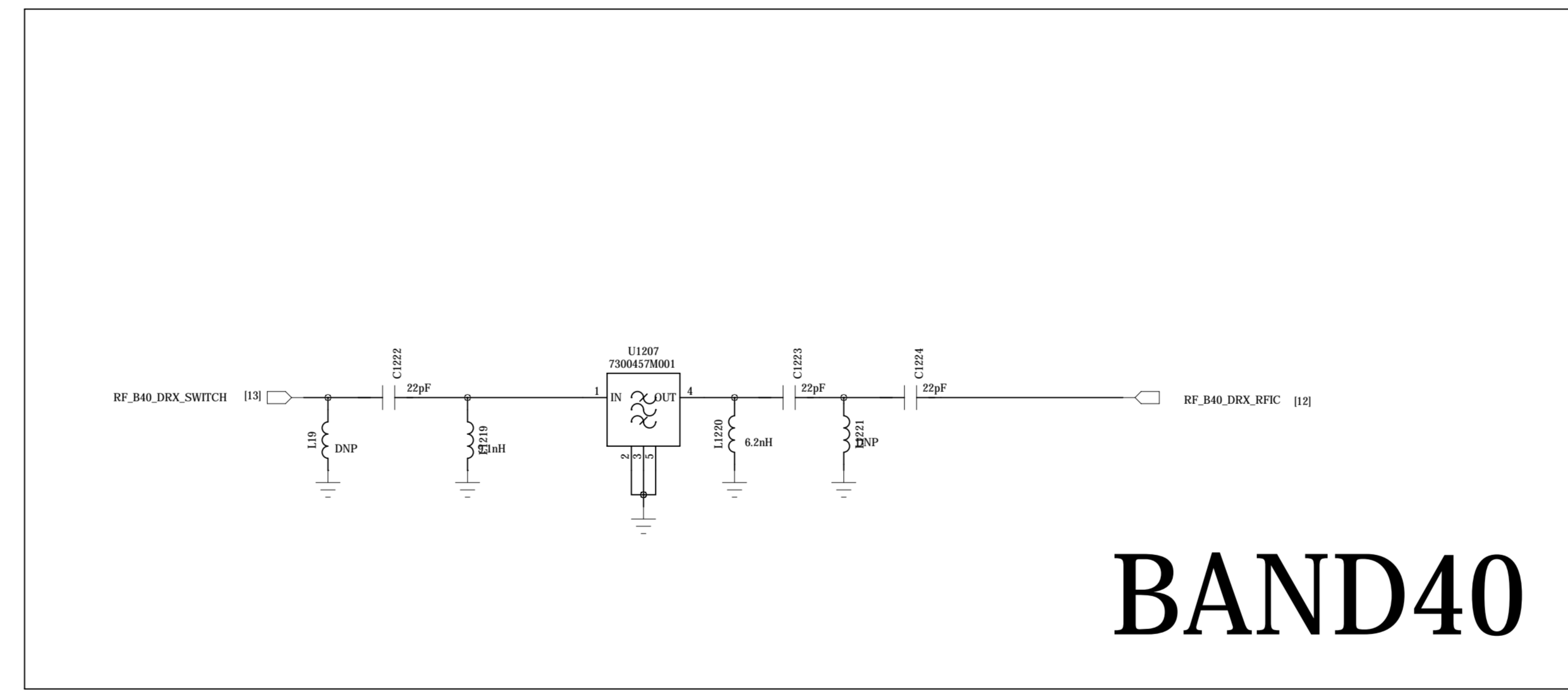
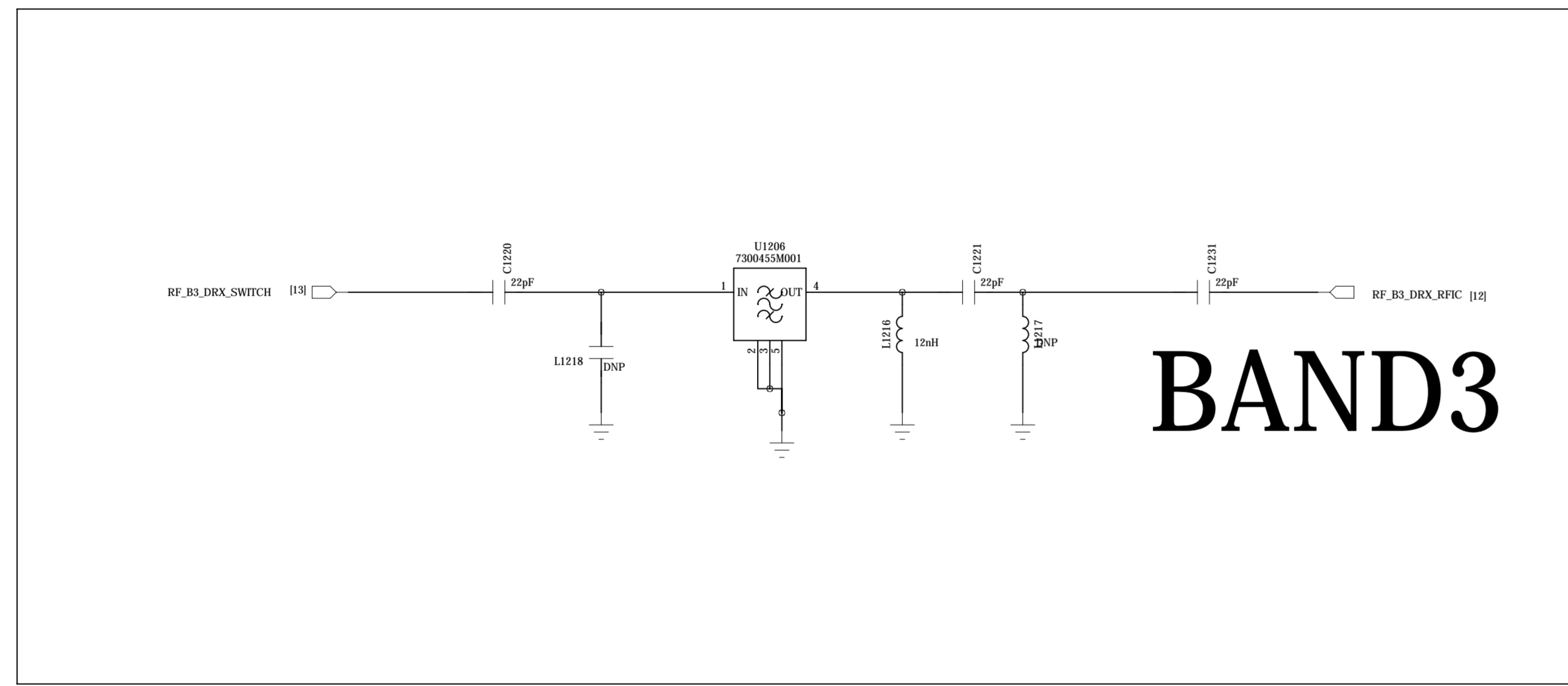
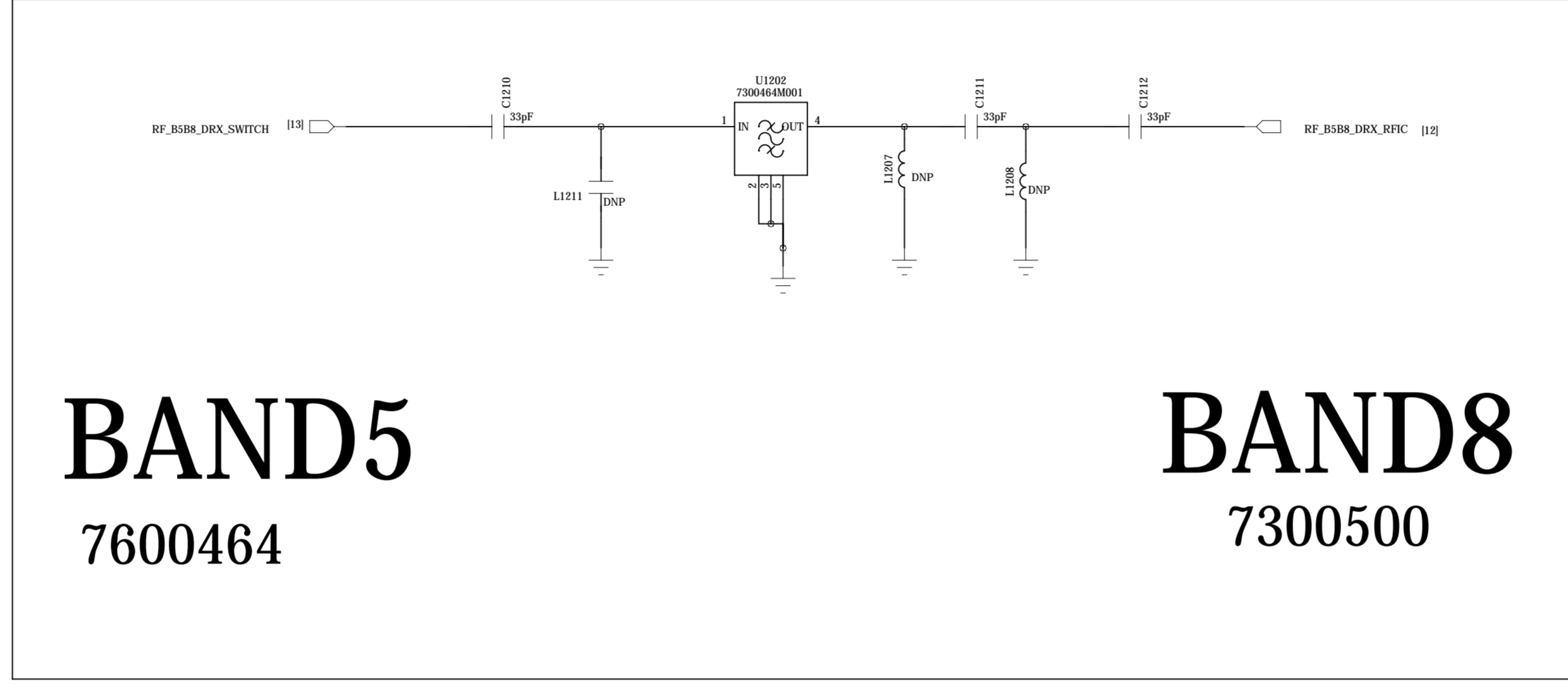
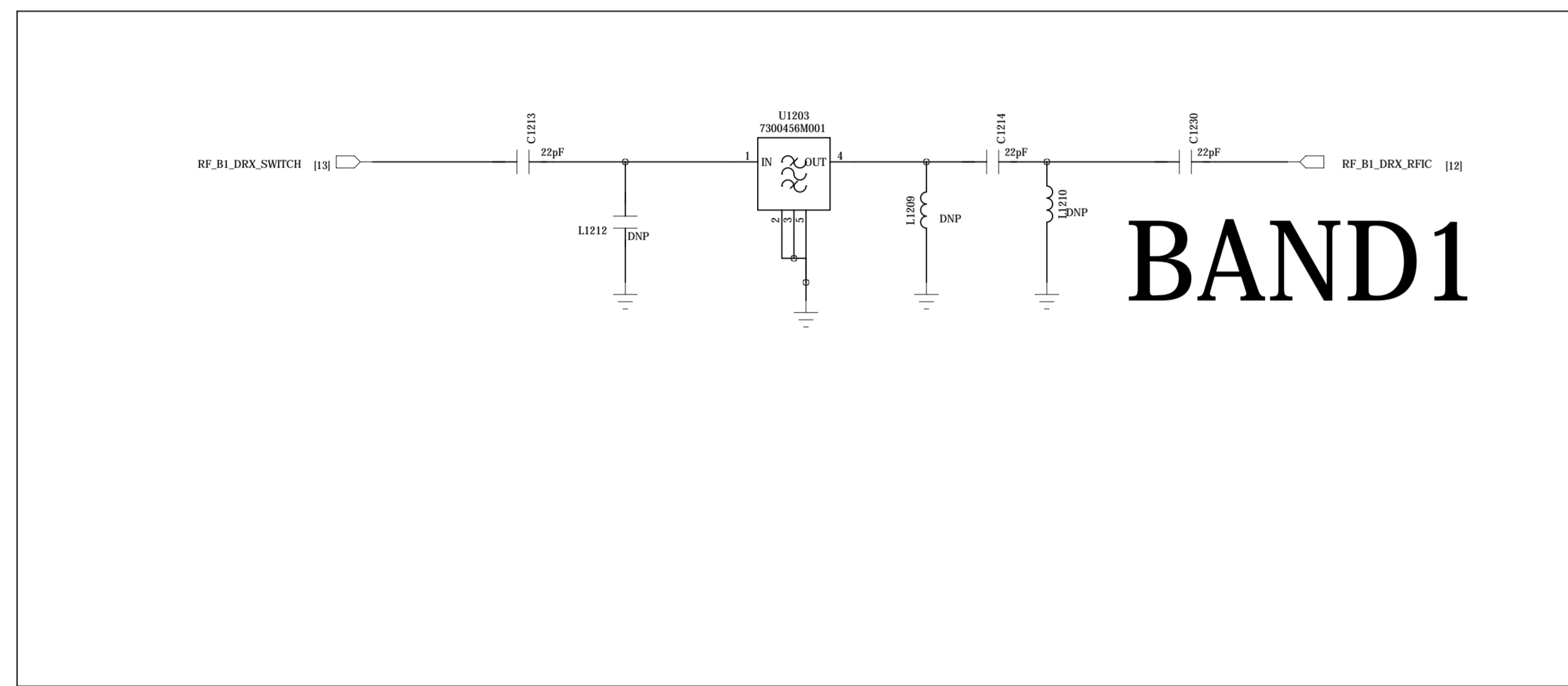
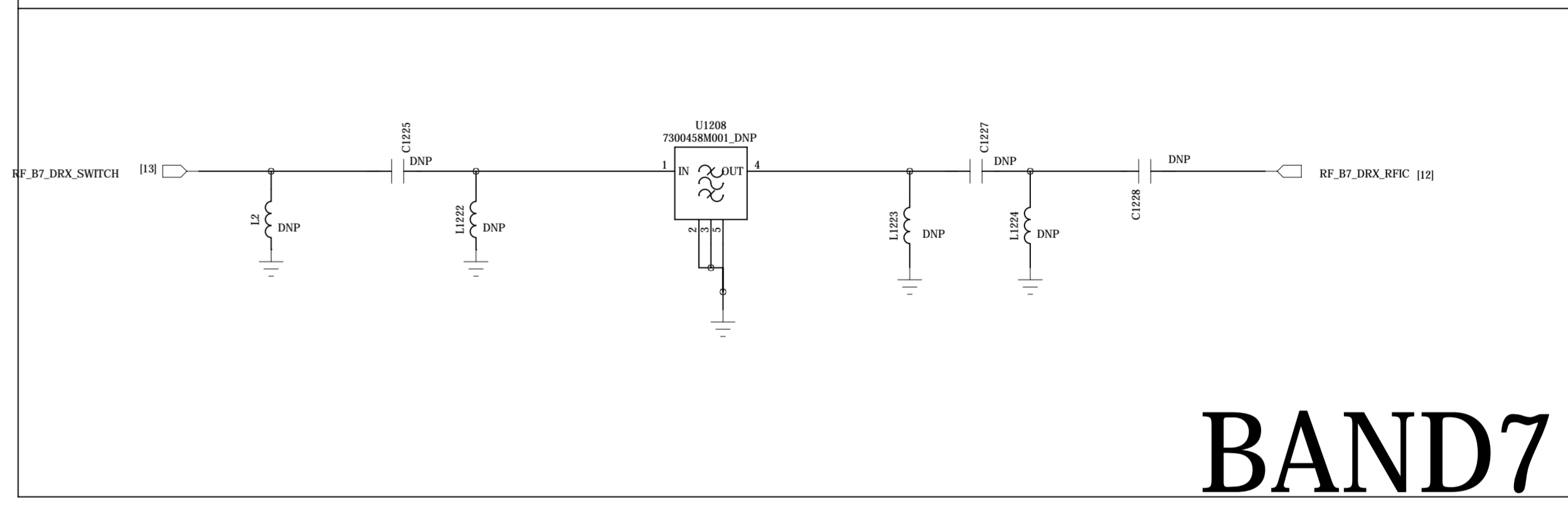
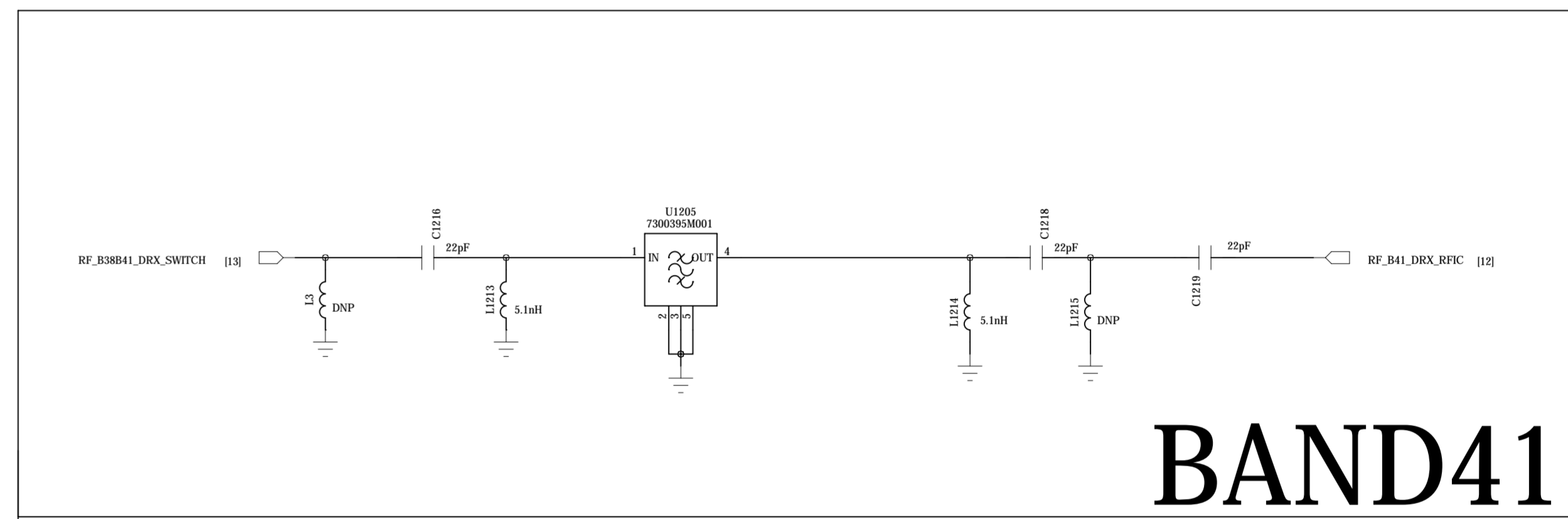
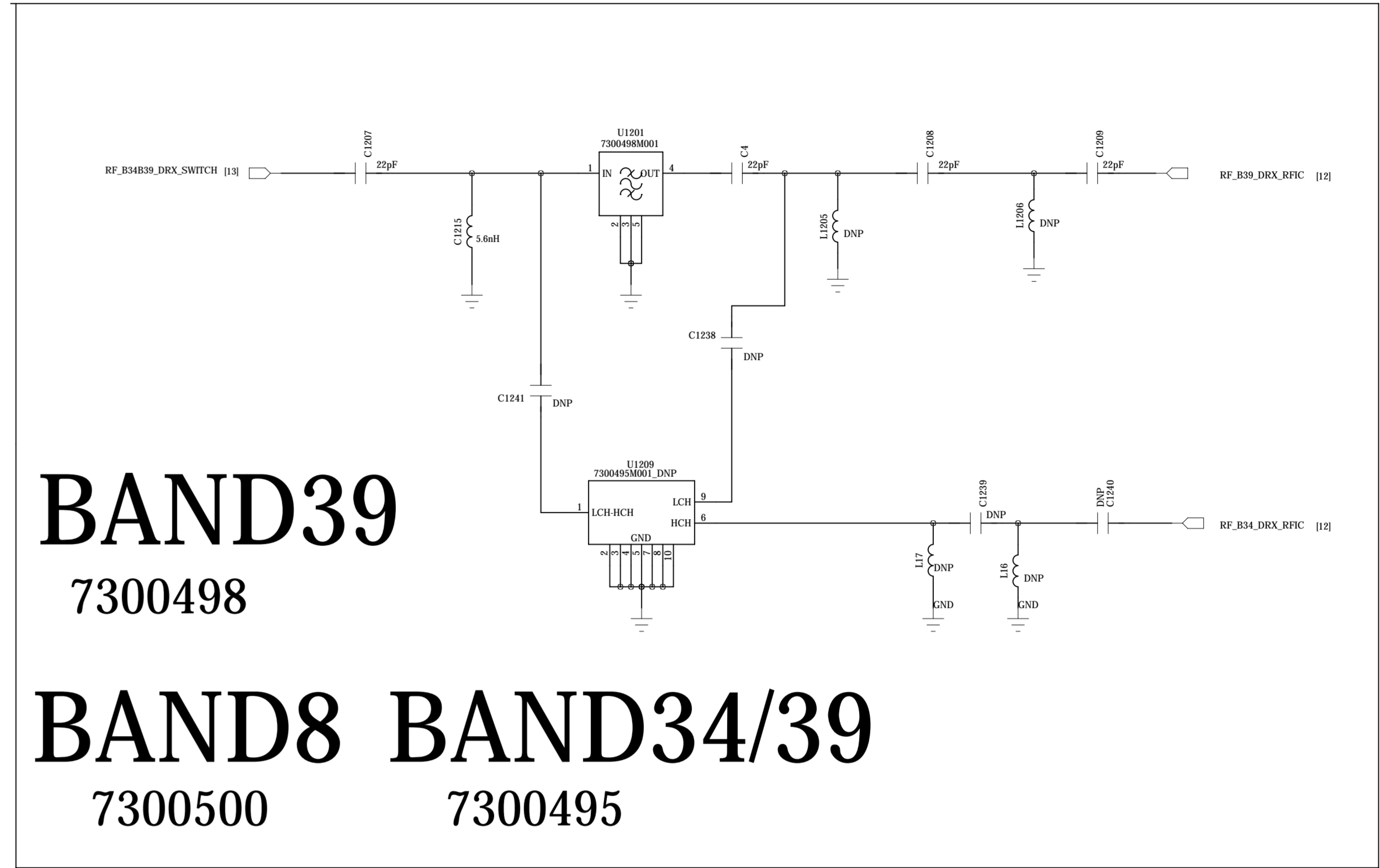
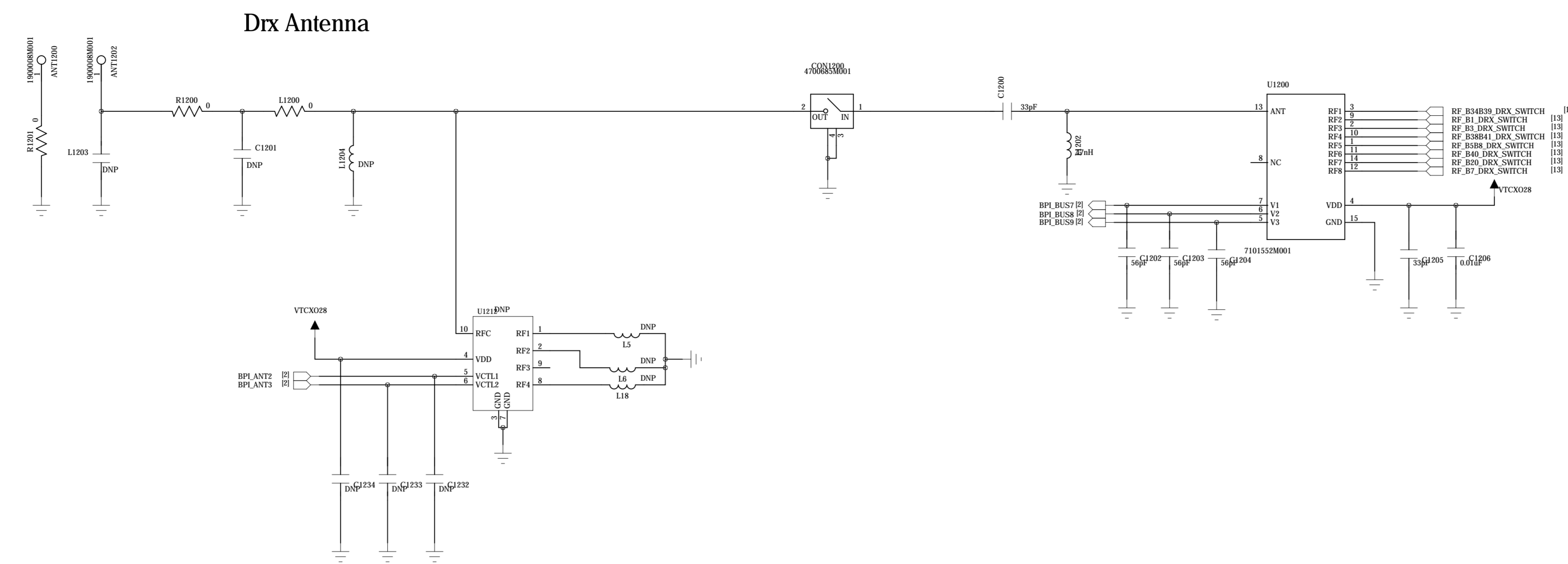
Note 31-1: close to PA, and located in the same layer

Power domain of MT6176



DRAWN		DATED		CODE		SIZE		DRAWING NO		REV	
CHECKED		DATED		SCALE		SHEET		OF		COMPANY	
QUALITY CONTROL		DATED		TITLE		DATE		APPROVED		DATE	
RELEASED		DATED		SCALE		SHEET		OF		COMPANY	

REVISION RECORD			
LTB	ECO NO.	APPROVED	DATE



DRAWN: <Drawn By>		DATE: <Drawn Date>		COMPANY: <Company Name>	
CHECKED: <Checked By>		DATE: <Checked Date>		TITLE: <Title>	
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		SCALE: <Scale>		REVISION: <Revision>	
				SHEET 48 13	