

# 2013 S-Series Intel Shark Bay

UMA/DIS Muxless Schematic  
14.0" Rampage 15.6" Renegade 17.0" Ricochet

Haswell-M Dual/Quad Core SV  
rPGA947 37W  
Lynx Point-M PCH

REV: MV

2013-08-01

*DY: No stuff*

*DIS\_PX: Only DIS install*

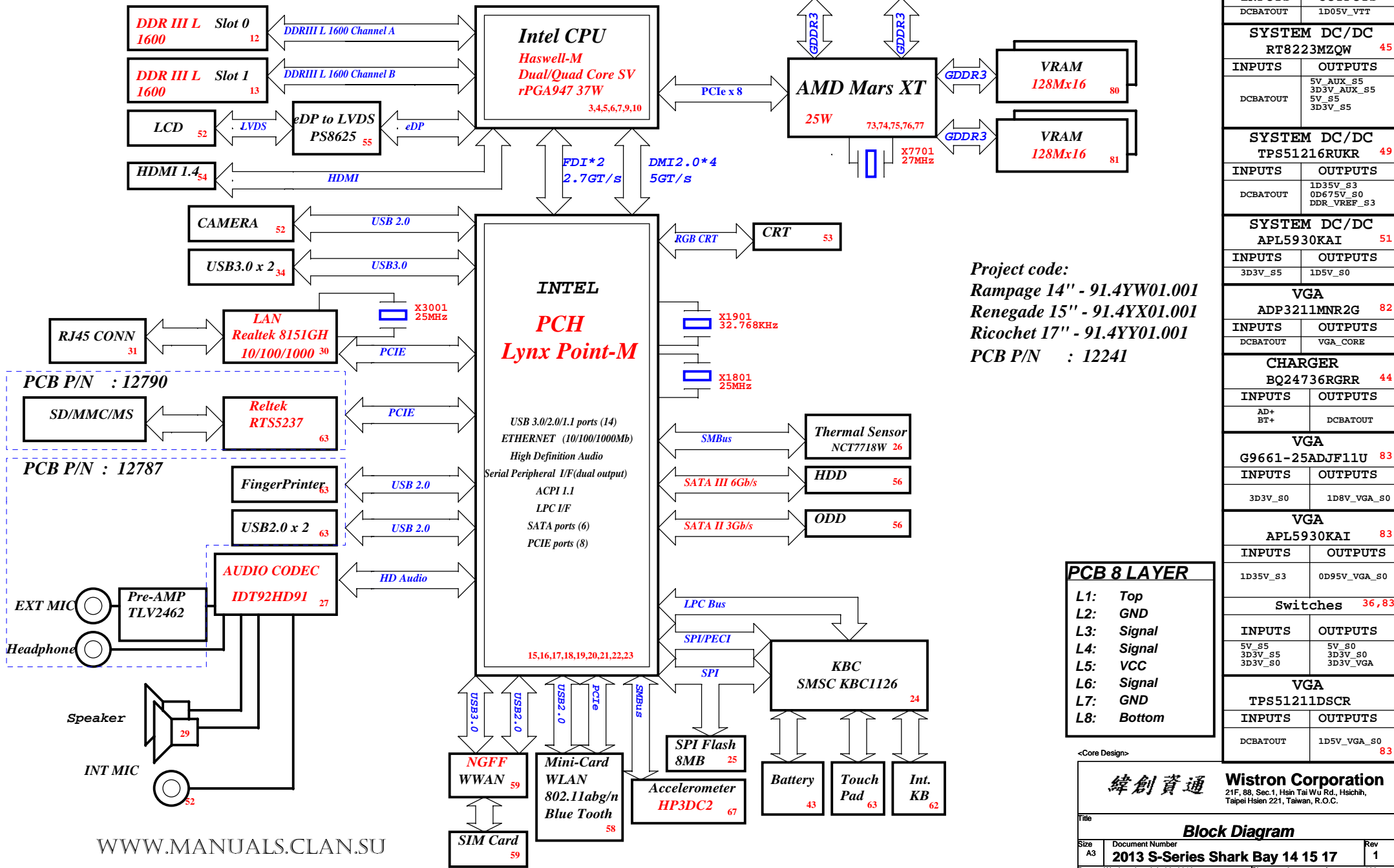
WWW.MANUALS.CLAN.SU

<Core Design>

<b>緯創資通</b>			<b>Wistron Corporation</b>		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>Cover Page</b>					
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# 2013 S-Series Intel Shark Bay 14.0" 15.6" 17.3"

(Muxless)



Project code:  
 Rampage 14" - 91.4YW01.001  
 Renegade 15" - 91.4YX01.001  
 Ricochet 17" - 91.4YY01.001  
 PCB P/N : 12241

**PCB 8 LAYER**

- L1: Top
- L2: GND
- L3: Signal
- L4: Signal
- L5: VCC
- L6: Signal
- L7: GND
- L8: Bottom

<b>CPU DC/DC</b> TPS51631RSMR 46,47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
<b>SYSTEM DC/DC</b> TPS51367RVER 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
<b>SYSTEM DC/DC</b> RT8223MZQW 45	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
<b>SYSTEM DC/DC</b> TPS51216RUKR 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3
<b>SYSTEM DC/DC</b> APL5930KAI 51	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
<b>VGA</b> ADP3211MNR2G 82	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
<b>CHARGER</b> BQ24736RGRR 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT
<b>VGA</b> G9661-25ADJF11U 83	
INPUTS	OUTPUTS
3D3V_S0	1D8V_VGA_S0
<b>VGA</b> APL5930KAI 83	
INPUTS	OUTPUTS
1D35V_S3	0D95V_VGA_S0
<b>Switches</b> 36,83	
INPUTS	OUTPUTS
5V_S5 3D3V_S5 3D3V_S0	5V_S0 3D3V_S0 3D3V_VGA
<b>VGA</b> TPS51211DSCR	
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0 83

<Core Design>

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Title: **Block Diagram**

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SSID = CPU

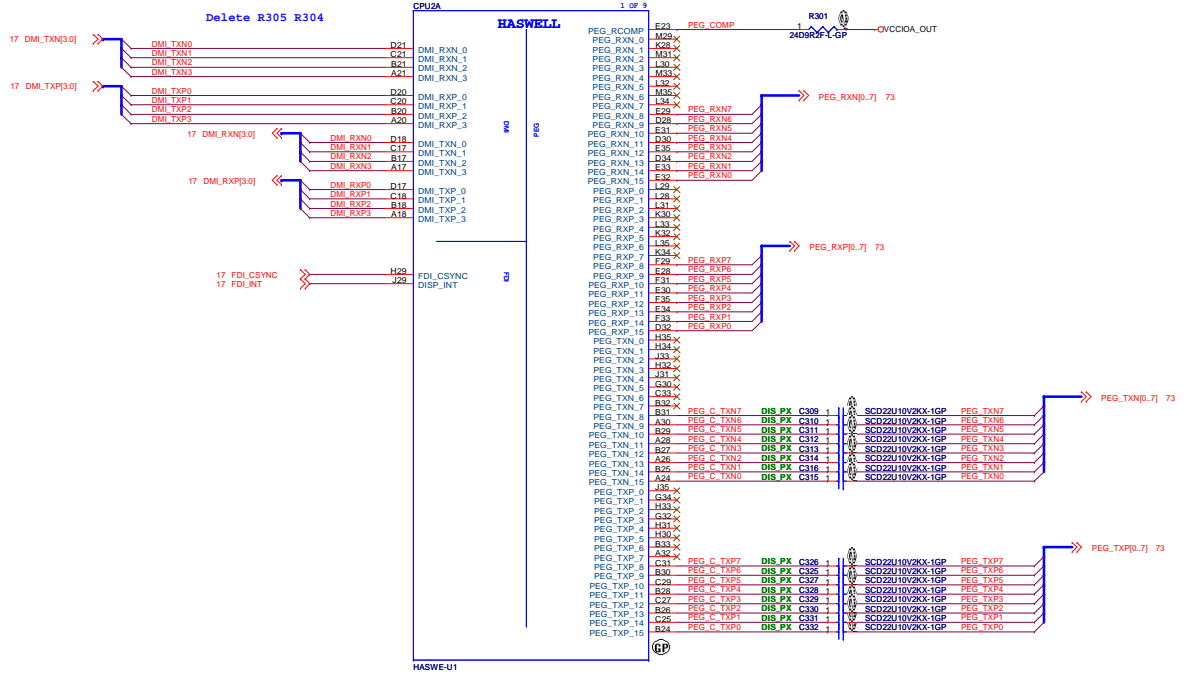
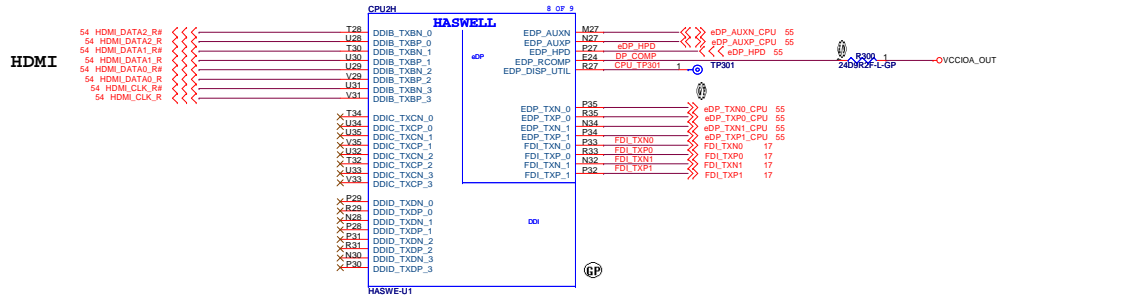


Table with 13 columns: Physical Link Matrix, Negotiated Link Matrix, Physical SMI Lanes Enable, and Processor. Rows include various CPU configurations and their corresponding link states.



«Core Design»

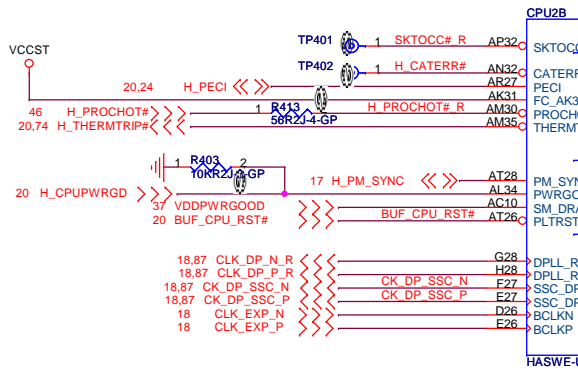
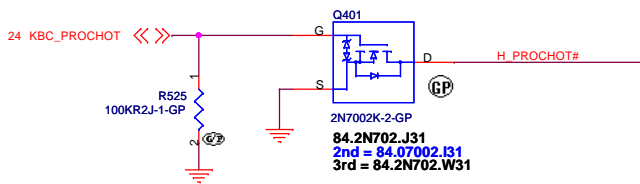
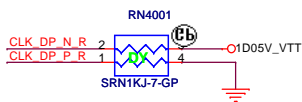
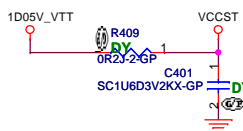
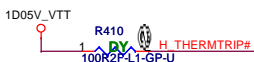
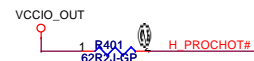
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Title: **CPU (PCIe/DMI/FDI)**

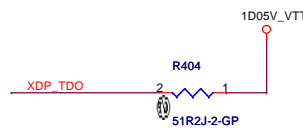
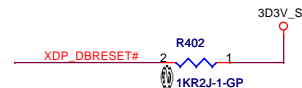
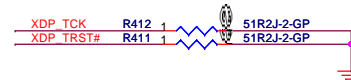
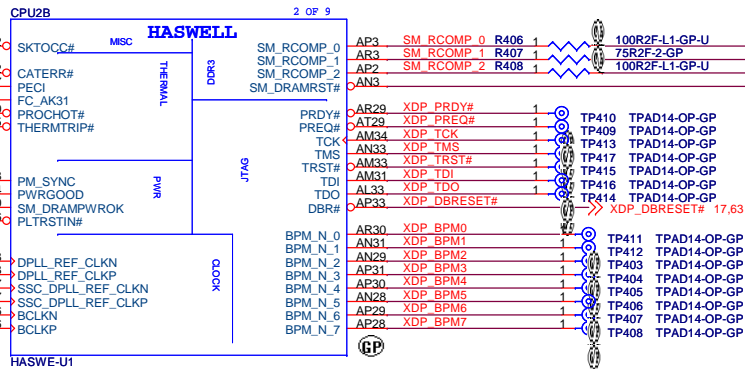
Size A2 Document Number: **2013 S-Series Shark Bay 14 15 17** Row 1

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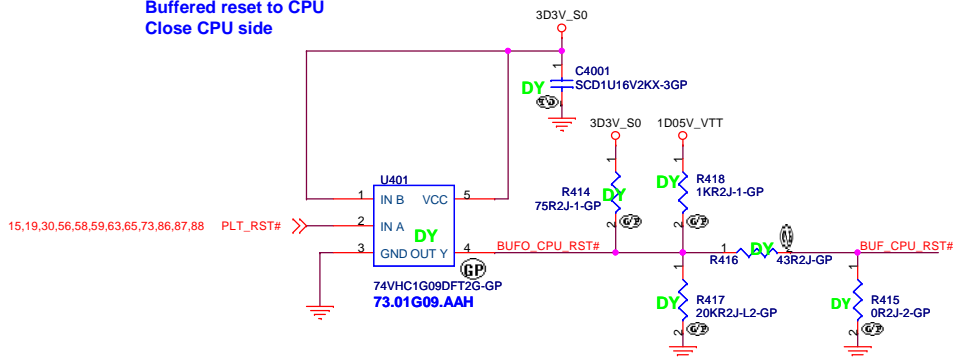
SSID = CPU



Signal Routing Guideline:  
SM\_RCOMP keep routing length less than 500 mils.



Buffered reset to CPU  
Close CPU side



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Title		
CPU (THERMAL/CLOCK/PM)		
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**SSID = CPU**

