Compal Confidential

DIS M/B Schematics Document

Haswell with DDRIII + Lynx Point PCH

MARS XT / SUN PRO

2013-04-18

LA-9641P

REV:1.0

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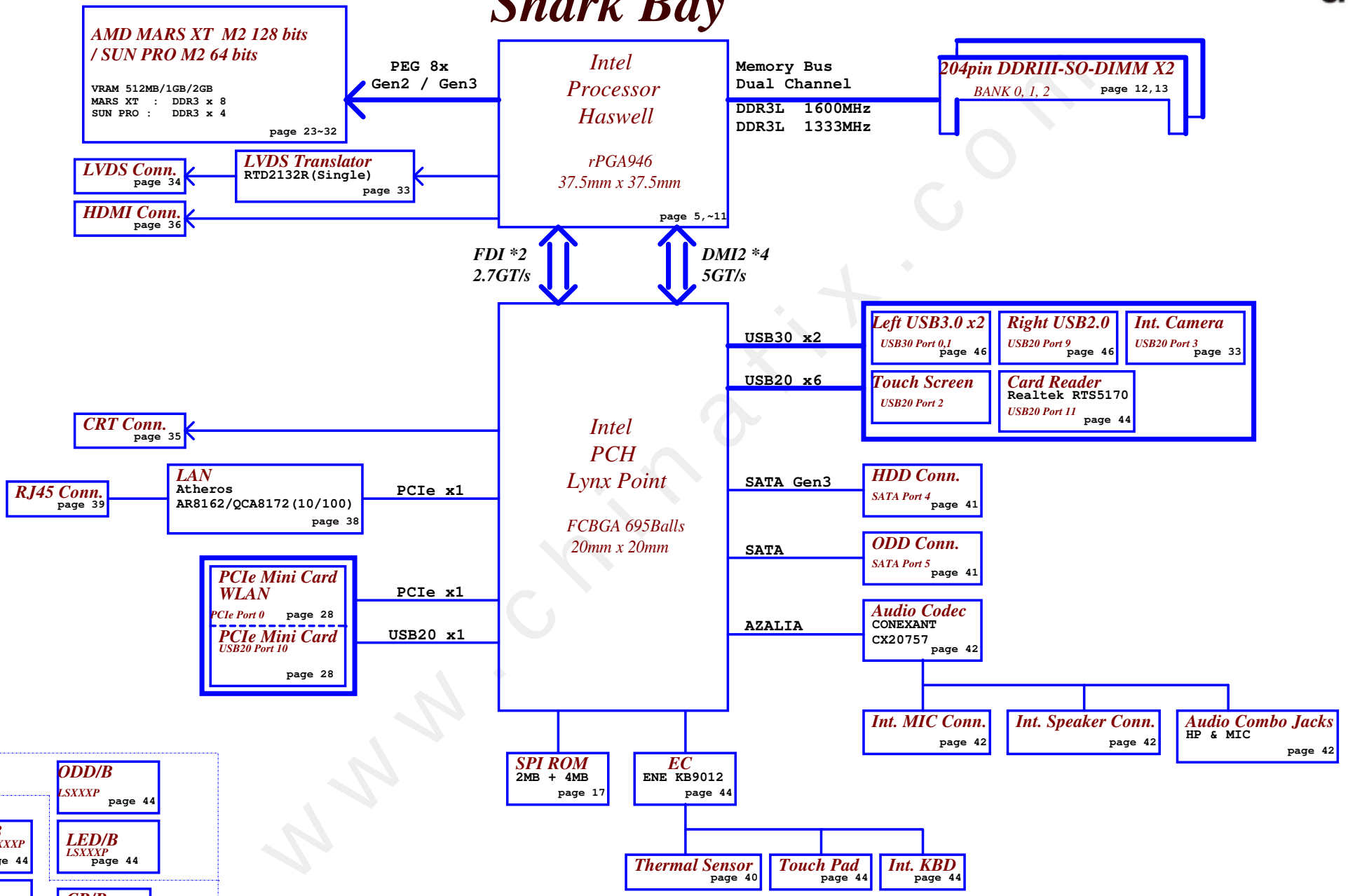
Compal confidential
File Name :

Shark Bay



Sub-borad

15"

14"

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Power/B
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LED/B
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USB/B
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Compal Electronics, Inc.			
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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS +VCC_CORE +VGA_CORE +1.5VS +0.675VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
	UHCI1	2	Touch screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	Right USB2.0
	UHCI5	10	WLAN
		11	Card reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
DIS	PX@
MARS XT	MARS@
SUN PRO	SUN@
HDMI	HDMI@
Deep S3	DS3@
NO Deep S3	NODS3@
8162 LAN	8162@
8172 LAN	8172@
LAN LDO MODE	LDO@
LAN SWR MODE	SWR@
LAN Surge	GAS@
USB30	USB30@
Cameara	CMOS@
LAN Switch mode	SWR@
Touch screen	TS@
Righ side USB	RUSB@
Zero ODD circuit	ZODD@
Share ROM	SROM@
Non-share ROM	NOSROM@
14"	14@
15"	15@
45 LEVEL	45@
X76 LEVEL	X76@
Unpop	@
AUDIO PART	MIC@
Connector	ME@

R_USB@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001_100xb

PCH SM Bus address

Device	Address
DDR DIMM1 ChannelA	0xA0
DDR DIMM2 ChannelB	0xA4

Device	Address
RTD2132R	1101 010Xb

AMD-GPU SM Bus address

Device	Address
Internal thermal sensor	1000_001xb

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X	V +3VS

VRAM BOM STRUCTURE Refer P4. VGA NOTE

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Title: Notes List

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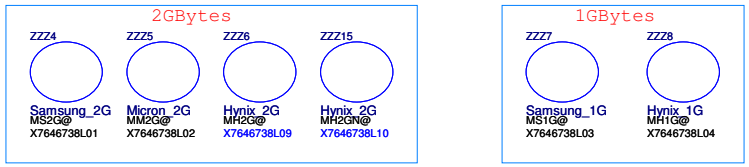
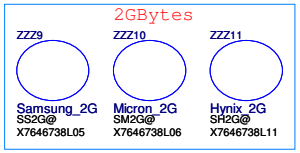
Mars XT VRAM STRAP

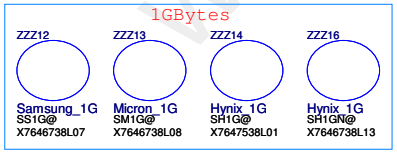
	Vendor (UV5, UV6, UV7, UV8 UV9, UV10, UV11, UV12)	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV20	X76@ R_pd RV27
ZZZ4 MS2G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	NC	4.75K
2GBytes ZZZ5 MM2G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	0	0	1	8.45K	2K
ZZZ6 MH2G@	Hynix 2048Mbits SA000065300 H5TQ2G63DFR-N0C	0	1	0	4.53K	2K
ZZZ7 MS1G@	Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	0	1	1	6.98K	4.99K
1GBytes ZZZ8 MH1G@	Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	1	1	1	4.75K	NC
2GBytes ZZZ15 MH2GN@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	1	0	0	4.53K	4.99K



Sun PRO VRAM STRAP

	Vendor (UV9, UV10, UV11, UV12)	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV20	X76@ R_pd RV27
ZZZ9 SS2G@	Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	NC	4.75K
2GBytes ZZZ10 SM2G@	Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-107G:E	0	0	1	8.45K	2K
ZZZ11 SH2G@	Hynix 4096Mbits SA00006DG00 256MX16 H5TQ4G63MFR-11C	0	1	0	4.53K	2K
ZZZ12 SS1G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	1	1	6.98K	4.99K
1GBytes ZZZ13 SM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	1	0	3.4K	10K
ZZZ14 SH1G@	Hynix 2048Mbits SA000065300 H5TQ2G63DFR-N0C	1	1	1	4.75K	NC
1GBytes ZZZ16 SH1GN@	Hynix 2048Mbits SA00006H400 H5TC2G63FFR-11C	1	0	0	4.53K	4.99K

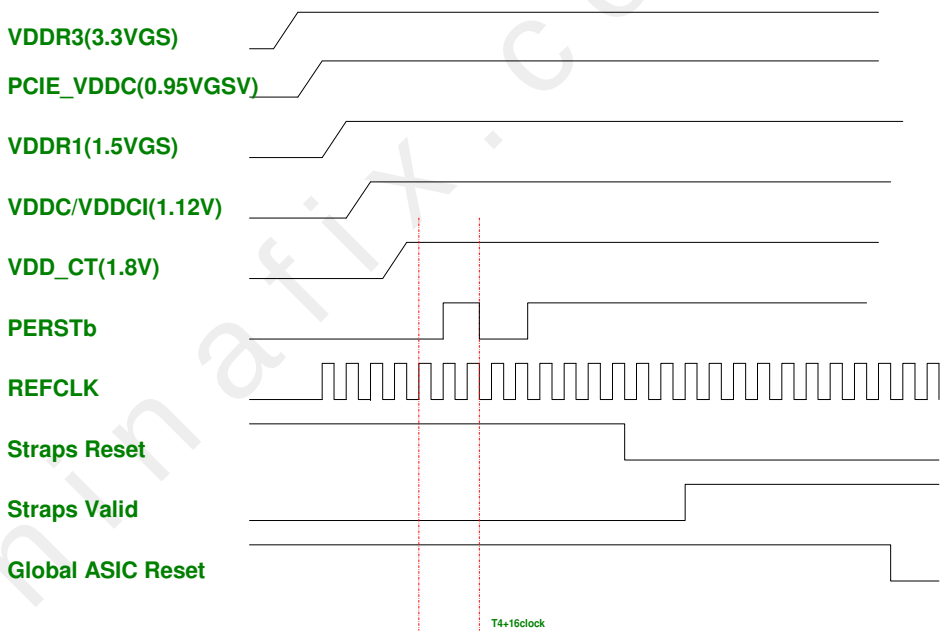




Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

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ZZZ1 14@

14" PCB LA9641

DA6000WQ000

ZZZ2 15@

15" PCB LA9641

DA6000WQ100

+VCOMP_OUT

PEG_RCOMP 2 — 24.9_0402_1% — 1 R1

Note:
Trace width=12 mils ,Spacing=15mils
Max length= 400 mils.

Haswell rPGA EDS

JCPU1A

<15> DMI_CRX_PTX_N0 — DMI_CRX_PTX_N0 D21 — DMI_RXN_0
<15> DMI_CRX_PTX_N1 — DMI_CRX_PTX_N1 C21 — DMI_RXN_1
<15> DMI_CRX_PTX_N2 — DMI_CRX_PTX_N2 B21 — DMI_RXN_2
<15> DMI_CRX_PTX_N3 — DMI_CRX_PTX_N3 A21 — DMI_RXN_3

<15> DMI_CRX_PTX_P0 — DMI_CRX_PTX_P0 D20 — DMI_RXP_0
<15> DMI_CRX_PTX_P1 — DMI_CRX_PTX_P1 C20 — DMI_RXP_1
<15> DMI_CRX_PTX_P2 — DMI_CRX_PTX_P2 B20 — DMI_RXP_2
<15> DMI_CRX_PTX_P3 — DMI_CRX_PTX_P3 A20 — DMI_RXP_3

<15> DMI_CTX_PRX_N0 — DMI_CTX_PRX_N0 D18 — DMI_TXN_0
<15> DMI_CTX_PRX_N1 — DMI_CTX_PRX_N1 C17 — DMI_TXN_1
<15> DMI_CTX_PRX_N2 — DMI_CTX_PRX_N2 B17 — DMI_TXN_2
<15> DMI_CTX_PRX_N3 — DMI_CTX_PRX_N3 A17 — DMI_TXN_3

<15> DMI_CTX_PRX_P0 — DMI_CTX_PRX_P0 D17 — DMI_TXP_0
<15> DMI_CTX_PRX_P1 — DMI_CTX_PRX_P1 C18 — DMI_TXP_1
<15> DMI_CTX_PRX_P2 — DMI_CTX_PRX_P2 B18 — DMI_TXP_2
<15> DMI_CTX_PRX_P3 — DMI_CTX_PRX_P3 A18 — DMI_TXP_3

DMI

<15> FDI_CSYNC — H29 — FDI_CSYNC
<15> FDI_INT — J29 — DISP_INT

FDI

Note:
Trace width=4 mils ,Spacing=5mil
Max length= 10000 mils.

PEG

PEG_RCOMP — E23 PEG_RCOMP

PEG_RXN_0 M29
PEG_RXN_1 K28
PEG_RXN_2 M31
PEG_RXN_3 L30
PEG_RXN_4 M33
PEG_RXN_5 L32
PEG_RXN_6 M35
PEG_RXN_7 L34
PEG_RXN_8 E29 PCIE_CRX_GTX_N7
PEG_RXN_9 D28 PCIE_CRX_GTX_N6
PEG_RXN_10 E31 PCIE_CRX_GTX_N5
PEG_RXN_11 D30 PCIE_CRX_GTX_N4
PEG_RXN_12 E35 PCIE_CRX_GTX_N3
PEG_RXN_13 D34 PCIE_CRX_GTX_N2
PEG_RXN_14 E33 PCIE_CRX_GTX_N1
PEG_RXN_15 E32 PCIE_CRX_GTX_N0 — PCIE_CRX_GTX_N[0..7] <23>

PEG_RXP_0 L29
PEG_RXP_1 L28
PEG_RXP_2 L31
PEG_RXP_3 K30
PEG_RXP_4 L33
PEG_RXP_5 K32
PEG_RXP_6 L35
PEG_RXP_7 K34
PEG_RXP_8 F29 PCIE_CRX_GTX_P7
PEG_RXP_9 E28 PCIE_CRX_GTX_P6
PEG_RXP_10 F31 PCIE_CRX_GTX_P5
PEG_RXP_11 E30 PCIE_CRX_GTX_P4
PEG_RXP_12 F35 PCIE_CRX_GTX_P3
PEG_RXP_13 E34 PCIE_CRX_GTX_P2
PEG_RXP_14 F33 PCIE_CRX_GTX_P1
PEG_RXP_15 D32 PCIE_CRX_GTX_P0 — PCIE_CRX_GTX_P[0..7] <23>

PEG_TXN_0 H35
PEG_TXN_1 H34
PEG_TXN_2 J33
PEG_TXN_3 H32
PEG_TXN_4 J31
PEG_TXN_5 G30
PEG_TXN_6 G33
PEG_TXN_7 B32
PEG_TXN_8 B31 PCIE_CTX_GRX_C_N7 — C9 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N7
PEG_TXN_9 A30 PCIE_CTX_GRX_C_N6 — C10 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N6
PEG_TXN_10 B29 PCIE_CTX_GRX_C_N5 — C11 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N5
PEG_TXN_11 A28 PCIE_CTX_GRX_C_N4 — C12 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N4
PEG_TXN_12 B27 PCIE_CTX_GRX_C_N3 — C13 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N3
PEG_TXN_13 A26 PCIE_CTX_GRX_C_N2 — C14 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N2
PEG_TXN_14 B25 PCIE_CTX_GRX_C_N1 — C15 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N1
PEG_TXN_15 A24 PCIE_CTX_GRX_C_N0 — C16 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N0 — PCIE_CTX_GRX_N[0..7] <23>

PEG_TXP_0 J35
PEG_TXP_1 G34
PEG_TXP_2 H33
PEG_TXP_3 G32
PEG_TXP_4 H31
PEG_TXP_5 G30
PEG_TXP_6 B33
PEG_TXP_7 A32
PEG_TXP_8 C31 PCIE_CTX_GRX_C_P7 — C25 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P7
PEG_TXP_9 B30 PCIE_CTX_GRX_C_P6 — C26 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P6
PEG_TXP_10 C29 PCIE_CTX_GRX_C_P5 — C27 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P5
PEG_TXP_11 B28 PCIE_CTX_GRX_C_P4 — C28 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P4
PEG_TXP_12 C27 PCIE_CTX_GRX_C_P3 — C29 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P3
PEG_TXP_13 B26 PCIE_CTX_GRX_C_P2 — C30 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P2
PEG_TXP_14 C25 PCIE_CTX_GRX_C_P1 — C31 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P1
PEG_TXP_15 B24 PCIE_CTX_GRX_C_P0 — C32 PX@ 1 — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P0 — PCIE_CTX_GRX_P[0..7] <23>

INTEL_HASWELL_HASWELL 1 OF 9

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